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An Experimental Verification of the Design Margin Analysis Method for Even-Stage Ring Oscillators with CMOS Latch

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1. Introduction

The ring oscillator circuit composed of CMOS inverters has been widely used due to its simple structure and its ability to operate at low-voltage. In the case of a conventional ring oscillator, continuity of oscillation is structurally secured since it is composed of an odd number of inverter chains. In odd-stage configurations, however, since it is difficult to generate 90-degree phase-shifted four-phase clock signals which are required for communication systems, Even-Stage Ring Oscillators (ESROs) comprising of even-numbered CMOS inverter chains with latches are used as shown in Fig. 1(a). Nevertheless, such circuits run the risk that oscillation may be stopped depending on the design parameters of each transistor, which clearly a problem. Focusing on the similarity between ESRO and SRAM circuit topologies as shown in Fig. 1(b), we suggested an analytical technique for quantitatively deriving design parameters which enable secure stable oscillation by applying the Static Noise Margin (SNM) analysis of SRAM circuits [1]. Based on this technique, the required condition for the ESRO to oscillate stably is that design must be performed within the region in which the three SNM values are all set to be positive as shown in Fig. 2. Our analysis technique, however, is based on the results of circuit simulations [1][2]. Verification by comparing measured data with simulated data has never been undertaken until now. Consequently in this study, we have aimed to verify the validity of the proposed theory by actual measurements of the ESRO TEGs.

2. Design and Measurement of ESRO

The circuit diagram of ESRO TEG we designed is shown in Fig. 3. Two inverters in the ESRO loop were substituted by Initial-voltage Preset-able Inverters (IPIs) which are capable of setting the initial node voltage. This enables the application of an initial voltage to the nodes, A1 and B1, externally by setting the NODESET signal. We designed a total of 45 types of ESROs by changing the gate width (W) values of the PMOS and NMOS circuits, within a range from one third to ten times the W value of the loop inverter. A photograph of a chip including the ESRO TEGs is shown in Fig. 4. Measurement results for each case; i.e. a case without the initial voltage setting, cases with initial voltages at HH, at LL and at HL, are shown in Fig. 5(a), (b), (c) and (d). In Fig. 5, a circle and a cross denote that oscillation was or was not recognized. According to Fig. 5(a), oscillation was recognized even in some circuits designed outside region A when a specific initial voltage was not set. Further, from the results in Fig. 5(d), the case with the initial voltage set at different levels for the HL condition, was the best case, with oscillation being recognized within the whole region which met the condition of WSNM > 0. On the other hand, when the initial voltage is set at HH (Fig. 5(b)) or LL (Fig. 5(c)), the design region capable of oscillating is limited to the region A + D or A + C. As a result, we experimentally confirmed that an ESRO designed within region A can only oscillate under any initial voltage condition that agrees well with the theory in reference [1].

3.Measurement of the Effect of Multiple Latches

Reference [2] shows that it is possible to improve design margins significantly by inserting multiple latches in the ESRO, and that oscillation is secured even if the latch circuit has a single-channel latch configuration either with the nMOS or pMOS circuits. To confirm this by measurement, we designed circuits equipped with multiple Variable-W Latch (VWL) circuits within the loop, as shown in Fig. 6. It is possible to increase or decrease the W value of the latch by inputting analog voltages into the two control terminals, pcont and ncont. A single-channel latch can be configured by setting pcont equal to Vdd or ncont to Gnd. Circuits with different design parameters, with multiple latches connected and with a single-channel latch configuration were realized using this single circuit by controlling the input level of pcont and ncont. The results of measurement are shown in Fig. 7. The boundary curve of SNM in Fig. 7 has also been obtained using the VWL SNM evaluation circuit shown in Fig. 6(c). When the number of latches to be used is multiplied, it has been confirmed through measurement that (1) the possible design area is limited to just within region A, as the design margin is not improved when inserting a second latch at an even stage after the first latch (LatchA + LatchC) as shown in Fig. 7(a), and that (2) the possible design area is greatly expanded to the region of A + D + C when inserting additional latches at the odd stages after the first latch (LatchA + LatchB) as shown in Fig. 7(b). The results totally corresponded to the theory described in reference [2].

4. Conclusions

The condition for oscillation of an even-stage ring oscillator has been confirmed in this study for the first time by actual measurements with the developed ESRO TEGs with IPIs. We also developed VWLs to achieve an ESRO with multiple latches and/or single-channel latch configurations. The results completely correspond to the

stable oscillation region of even-stage ring oscillators based on the SNM analysis technique of the SRAM we have proposed in the past.

Acknowledgments

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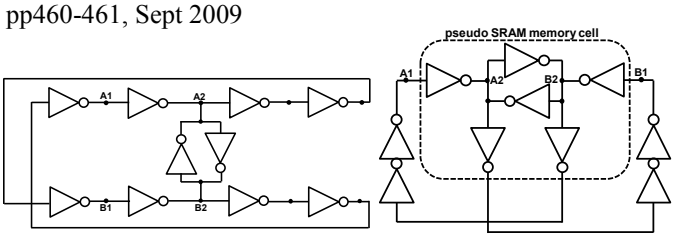
References

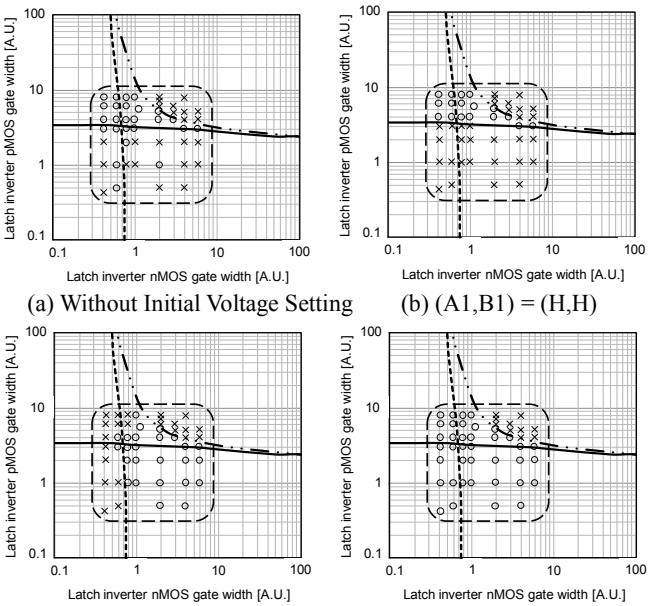
[1] K. Nakamura et al., *Extended Abstract of 2008 SSDM*, pp. 480-481, Sept 2008

[2] Y. Kohara et al., *Extended Abstract of 2009 SSDM*, pp460-461, Sept 2009



(a) Even-Stage Ring Oscillator (b) Pseudo SRAM memory cell

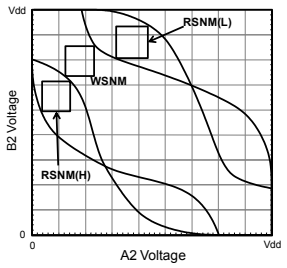
Fig.1 ESRO Circuit Diagrams

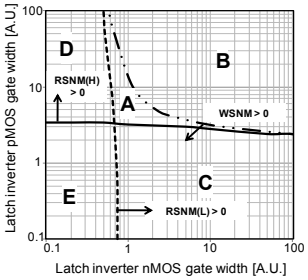


(a) Without Initial Voltage Setting (b) (A1,B1) = (H,H)

(c) (A1,B1) = (L,L) (d) (A1,B1) = (H,L)

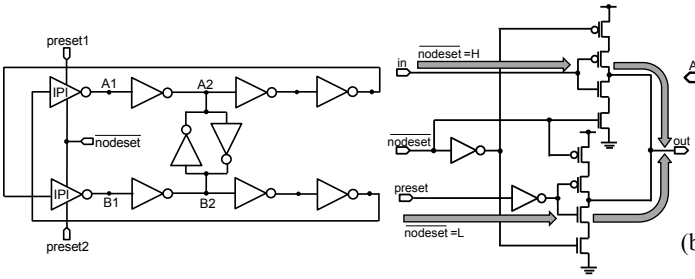
Fig.5 Measured Results of ESRO with IPIs





(a) Three SNMs (b) Design Margin Diagram

Fig.2 Design Margin of ESRO with SNM Analysis



(a) ESRO with IPIs (b) Initial-voltage Preset-able Inverter(IPI)

Fig.3 Developed ESRO for Measurement

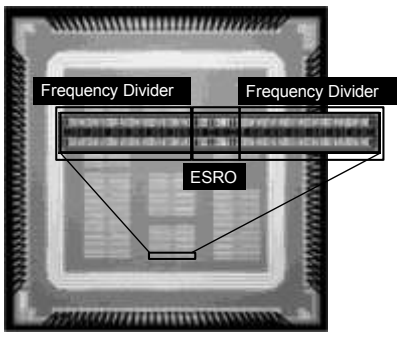
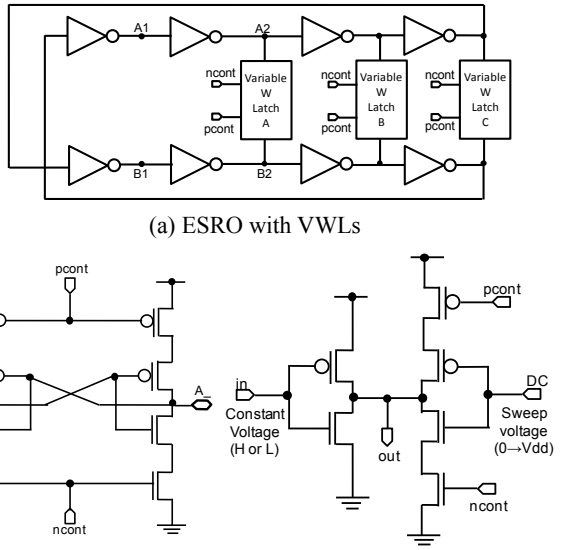
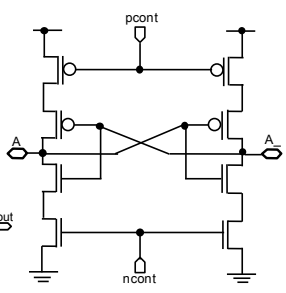


Fig.4 Chip Photograph

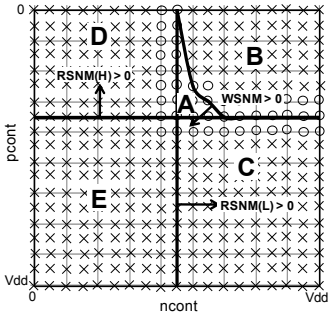


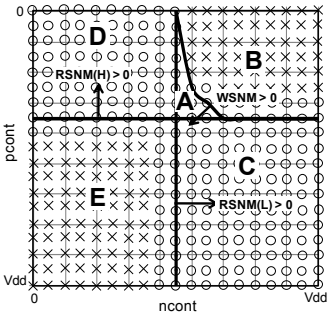
(a) ESRO with VWLs



(b) Variable W Latch(VWL) (c) VWL for SNM Measurement

Fig.6 ESRO with Multiple or Single-Channel Latch





(a) LatchA + LatchC (b) LatchA + LatchB

Fig.7 Measured Results of ESRO with VWLs