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MOS Power Cells for Output Power Levels of 17 to 23 dBm

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1. Introduction

Because the scaling-down of the channel length in the deep-submicrons CMOS process, the reliability issues have emerged, especially for high power applications. The degradation of dc and RF characteristics is induced by the hot-carrier effect [1], [2], which is more serious in nMOSFETs than in pMOSFETs due to the smaller energy barrier and longer mean-free-path of electrons [3]. Nevertheless, NMOS power cells are preferred in RF power amplifier (PA) design because of their higher current-driving capabilities. It is very important to design a power cell with high power-added efficiency (PAE), high power gain, good linearity and reliability. But these performances are influenced by the non-ideal effects including thermal effects associated with the thermal coupling between sub-cells, and depend on the geometry of the designed power cells [4]. In general, in order to do the reliability test of MOSFETs, RF stress was induced under the accelerated stress condition with much larger values of V_D or V_G [5]. In [6], the performance degradation of power cells with power capacity of 17dBm due to hot-carrier effect and oxide soft breakdown has been investigated. In [7], [8], the performance degradation of power cells with power capacity of 17dBm due to output mismatch has also been studied. In this work, the power cells under investigations were designed for maximum output power level at 17 dBm, 20dBm, and 23 dBm, corresponding to 50 mW. By the extension of layout pattern with a multiply of 2, the power capacity was investigated.

2. Designed Cells

In this work, nMOS transistors were fabricated by using a 0.18 triple-well 1P6M CMOS process. Fig. 1 shows the photographs of three designed cells. The power cell of cell I consists of four dispersive 16-finger transistor modules connected in parallel with the distance of 15mm. In both cells, the channel length is 0.18mm and the total channel width is 320mm. Designed cells were biased at V_{GS} of 1.2 V and V_{DS} of 1.8 V expect that the cell III was biased at V_{GS} of 1.2 V and V_{DS} of 2.2 V in order to enhance output power. These cells were biased for class A operation (i.e. at 50% of dc). The size and bias condition of the cells were designed to implement output power of 17 dBm. The power cell II is the extended structure of the cell I by laterally copying the layout pattern of the cell I. The maximum output power of the cell II should ideally be doubled that of cell I due to two times the number of transistors. Similarly, the power cell III is the extended structure of the cell II by vertically copying the layout pattern of the cell II. The power cells II and III were designed to implement output power of 20dBm and 23dBm, respectively.

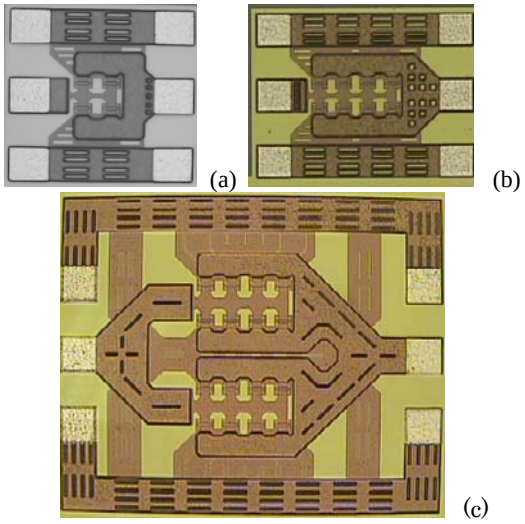

Fig.1 Photograph of the designed power cells: (a) cell I for 17dBm, (b) cell II for 20dbm and (c) cell III for 23 dbm.

The on-wafer dc characteristics were measured by using Agilent 4142B. The power measurements were carried out by using Agilent 8241A signal generator and Anritsu ML2438A power meter. The load-pull measurement for the maximum output power match was done by MAURY 982B01 tuners. The measurement for the power cells was done at 5.2 GHz or 2.4GHz.

Fig.1 shows the plot of output power (P_{out}) and power added efficiency (PAE) versus input power (P_{in}). All measurements were done under the optimum output matching condition. At 5.2GHz, the maximum output power is about 18.2 dBm with PAE of 24.9%, 21.5dBm with PAE of 49.2%, and 22dBm with PAE of 11.2% for the cell I, cell II, and cell III, respectively. It is observed that the output power of the cell I can achieve the wanted 17dBm, but the soft breakdown occurs when output power increase over 18.2dBm. The drain voltage would reach to the maximum acceptable value when the output power exceeded the limit

of power capacity of the studied cell. At this situation, the electric field E_{DG} between drain and gate would accelerate the soft breakdown. The output power of the cells II can also achieve the wanted 20dBm and soft breakdown does not occur when output power is increased to 21.45 dBm. The output power of the cell III can not achieve the wanted 23dBm but nearly saturate to 21.91 dBm or so and the PAE is smaller. For the cell III, the power performance at 2.4GHz was also measured. The output power can achieve 25.30 dBm. This means that the transistor size of the cell III is enough to generate output power more than 23 dBm. For the cell III, the layout parasitic of the large-area metal line and device parasitic capacitance at the drain terminal results in the smaller output power capacity for higher-frequency signals. Table I list the cut-off frequency (f_T) of the three cells. The f_T indeed decreases with the increase of transistor size of power cell due to the increased parasitic parasitic at drain.

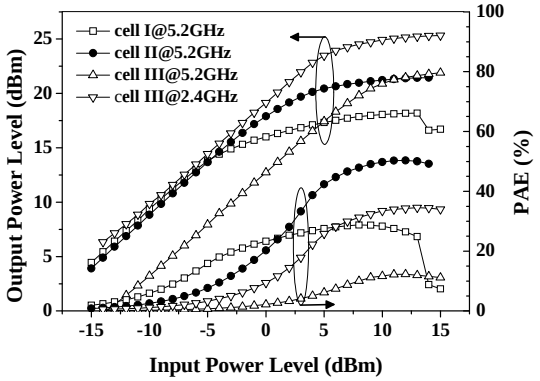

Fig.2 Performances of the three kinds of power cells at 5.2 GHz or 2.4GHz.

Table I The cut-off frequency of the three cells

Power cell	Cell I	Cell II	Cell III
Designed P_{out}(dBm)	17	20	23
F_T(GHz)	60	48	20

To enhance the power capacity, an extra cell (cell IV) was designed to achieve output power of 23 dBm. Fig.3 show the layout pattern of the cell IV. The main difference between the cells III and IV is the distance between rows of power modules. The cell IV has larger spacing between rows. Fig.4 shows the measured the plot of output power versus input power at 2.4 GHz. It is observed that the maximum output power is 25.43 dBm, but soft breakdown occurs. Larger spacing of power modules results in alleviated thermal effect and hence the cell has slightly larger output power, but the power level just arrives at the limit of soft breakdown. At 5.2 GHz, the output power is 22.1 dBm, which is still smaller than the wanted 23 dBm.

3. Conclusions

The output power capacity of power cells with two and four times the referenced power cell, which can achieve the output power capacity of 17 dBm, has been investigated. When the transistor size of power cell increase up to a certain size, e.g. that of cell III, the output power can not proportionally increase with the increase of transistor size due to parasitic capacitance even though the thermal effect is alleviated by expanding spacing between power modules. In addition, the cut-off frequency also decreases due device and layout paracitics. Soft breakdown can occur at higher output levels.

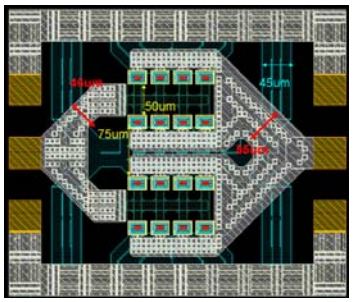

Fig.3 The layout pattern of the cell IV.

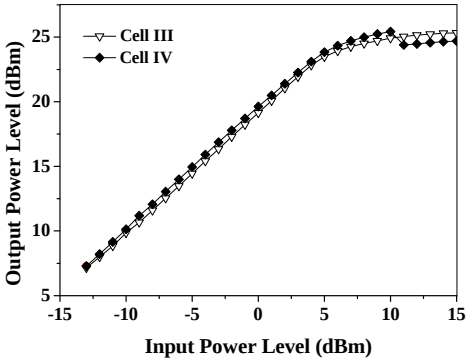

Fig.4 Power performance of the cells III and IV.

Acknowledgements

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