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SPICE MOSFET Analog Model Parameter Verification and Re-optimization Based on g_m/I_D Lookup Table Design Methodology

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1. Introduction

Deployments of wireless and wireline systems demand high-performance and low-cost mixed-signal SoCs in scaled CMOS technologies. Short channel effects in scaled CMOS increases the complexity in SPICE MOSFET models, and the increased variability in CMOS process requests careful attentions in the task of model parameter extraction. Since the conventional model parameter extraction and variability analysis are primarily based on digital circuits, such as transistors, ring oscillators and SRAM [1], verification and re-optimization methods of analog characteristics between simulations and measurements should be established to avoid unpredicted yield loss. For the contribution to the enhanced design productivity, this verification process should be closely related to the state-of-the-art analog design methodology.

2. Verification Method of Analog Model Parameters

g_m/I_D design methodology acts as a transistor sizing tool for low-power designs since g_m/I_D, the ratio of transconductance g_m over drain current I_D, can specify the all device operation regions from strong to weak inversion regions [2]. Lookup tables, representing the relationship between overdrive voltage V_{ov} and g_m/I_D, and transit frequency f_T, intrinsic gain g_m/g_{ds}, where g_{ds} is the output conductance of a transistor, and current density I_D/W as a function of g_m/I_D for various Ls, are generated by SPICE corner simulations for the worst-case design of analog circuits [3]. 0.18µm nMOS transistor simulation results including typical and corner conditions as well as the measurement results obtained from DC and RF measurements of a test chip are plotted for each technology metric of g_m/I_D lookup tables in Fig. 1. Die micrograph and organization of the test chip with nMOS and pMOS transistors with various Ls ranging from 0.18µm to 0.44 µm as well as de-embedding patterns for f_T measurement are presented in Fig. 2.

From Fig. 1, notable disagreements between the simulations and measurements are observed in f_T and I_D/W plots. The disagreement in g_m/I_D lookup tables is quantitatively evaluated by the error index $Err(L)$ for each L, as given in (1) and (2), and $Err(L)$s for original and after re-optimization are summarized in Table I, where $Err(L)$ over 10% is highlighted. The average value of original $Err(L)$ is calculated as 15.1%, and this disagreement results the underestimation of OTA settling time around 18%.

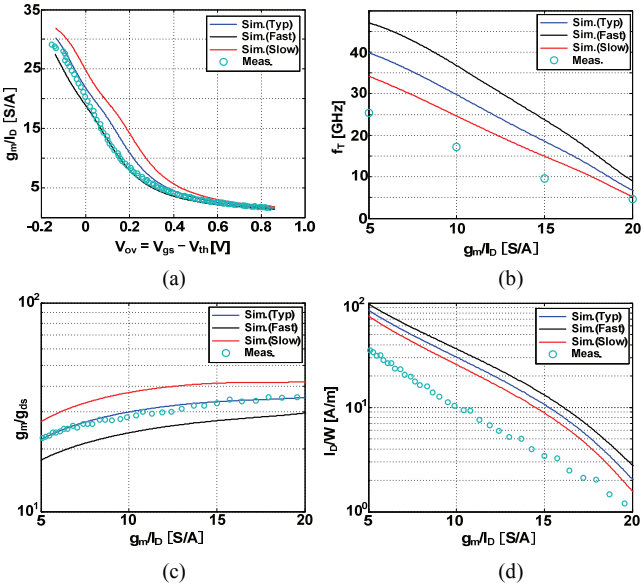


Fig.1 Simulation and measurement results of g_m/I_D plots for 0.18µm nMOS transistor. (a) V_{ov} vs g_m/I_D, (b) f_T, (c) g_m/g_{ds}, (d) I_D/W.

Fig. 2 Test chip die micrograph and its organization.

Therefore, it is concluded that MOSFET analog parameters should be re-optimized.

$$Err(L) = \frac{100}{\left(\frac{g_m}{I_D}\right)_{max} - \left(\frac{g_m}{I_D}\right)_{min}} \int_{\left(\frac{g_m}{I_D}\right)_{min}}^{\left(\frac{g_m}{I_D}\right)_{max}} \left| f\left(\frac{g_m}{I_D}\right) \right| d\left(\frac{g_m}{I_D}\right) \quad (1)$$

$$f = \begin{cases} \dfrac{X_{meas} - X_{sim,max}}{X_{sim,max}} & (\text{if } X_{meas} > X_{sim,max}) \\ 0 & (\text{if } X_{sim,max} \geq X_{meas} \geq X_{sim,min}) \\ \dfrac{X_{meas} - X_{sim,min}}{X_{sim,min}} & (\text{if } X_{meas} < X_{sim,min}) \end{cases} \quad (2)$$

Table I Error indices $Err(L)$ before and after re-optimization

<Original (before re-optimization)>

Gate Length [μm]		0.18	0.28	0.36	0.44
nMOS	g_m/I_D	0.0	0.0	0.0	0.1
	f_T	29.2	25.7	27.6	28.1
	g_m/g_{ds}	0.0	6.3	38.5	49.9
	I_D/W	24.1	26.8	28.6	29.4
pMOS	g_m/I_D	0.5	0.7	1.1	1.6
	f_T	8.6	13.3	9.0	7.4
	g_m/g_{ds}	0.0	5.4	4.1	2.1
	I_D/W	22.4	26.8	31.1	33.1

<After re-optimization>

Gate Length [μm]		0.18	0.28	0.36	0.44
nMOS	g_m/I_D	0.0	0.0	0.0	0.0
	f_T	5.3	3.9	4.8	5.4
	g_m/g_{ds}	0.0	9.4	13.2	18.3
	I_D/W	1.6	0.2	0.5	0.7
pMOS	g_m/I_D	0.0	0.0	0.0	0.0
	f_T	0.0	0.5	3.5	6.9
	g_m/g_{ds}	0.0	6.4	3.5	1.4
	I_D/W	0.0	0.0	0.0	0.0

3. Re-optimization of MOSFET analog parameters

The analog parameter re-optimization sequence is presented in Fig. 3. Primary guidelines of the re-optimization are 1) minimizing the number of re-optimized parameters and 2) minimizing the influences to digital characteristics. Disagreements typically indicate dependencies on g_m/I_D and L. If disagreements are observed where g_m/I_D is over 15 as shown in Fig. 4, which occurs in a pMOS transistor with L=0.18μm, subthreshold parameters are to be calibrated. From a sensitivity analysis, only voff (offset voltage in subthreshold region) is optimized to fit simulated f_T and I_D/W curves to the measurements. Subsequently, as shown in Fig. 1 (a), measurement values of g_m/I_D is not located on the typical value of the simulation due to the process perturbation. To compensate this perturbation, g_m/I_D values in each g_m/g_{ds}, f_T and I_D/W curve are shifted in order to set measured g_m/I_D values onto typical simulated lines in the V_{ov} vs g_m/I_D plots (g_m/I_D compensation).

The following calibration strategy is determined from the parameter sorting table, as shown in Table II, presenting the correlation between SPICE parameters and g_m/I_D metrics. Generic parameters are not calibrated since they influence all metrics. Parameters related to g_m/g_{ds} are independent of f_T and I_D/W; as the results, disagreement in g_m/g_{ds} vs L curve is calibrated in advance as shown in Fig. 5 (a), where only pdiblc2 (DIBL correction parameter) is optimized after comparing $Err(L)$ sensitivities from other parameters. Disagreements in f_T and I_D/W curves are calibrated with the common parameters in Table II, and from $Err(L)$ sensitivity analysis only b0 (bulk charge effect coefficient) is optimized. The impact of digital characteristics through the re-optimization is evaluated by the relative change of 11-stage ring oscillator delay t_d as shown in Table III. Calibrations for the subthreshold and g_m/g_{ds} disagreements do not influence the delay as is expected; however f_T calibration shifts t_d since f_T is inversely proportional to t_d from the first order analysis. After the entire re-optimization process, $Err(L)$ is reduce to the values as shown in Table I, and the averaged $Err(L)$ becomes 2.7%. The remained $Err(L)$ is not caused by the re-optimization restriction but the corner model inaccuracy.

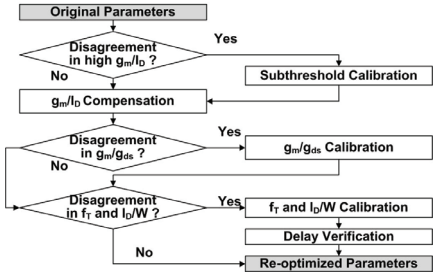


Fig. 3 Sequence of MOSFET analog parameter re-optimization.

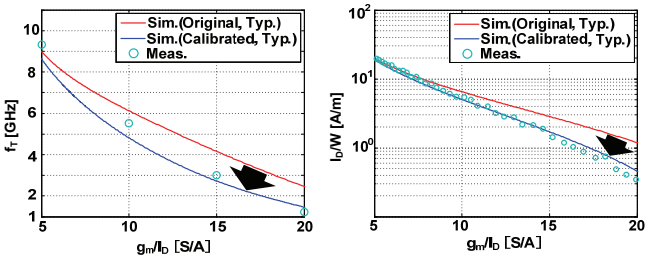
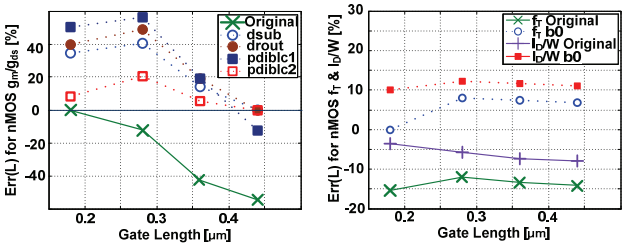


Fig. 4 Subthreshold calibration to disagreement in high g_m/I_D region (pMOS transistor with L=0.18μm).

Table II MOSFET analog parameter sorting table

	f_T	g_m/g_{ds}	I_D/W
f_T	xpart, clc, dlc,...	(No Parameter)	b0 , ags, nlx, ...
g_m/g_{ds}		dsub, pdiblc1, ..	(No Parameter)
I_D/W			wl, wwl, ...
Generic Parameters	u0, ua, ub, vsat, a2, rdsw, ... (Not to be calibrated)		



(a) (b)

Fig. 5 Calibration to (a) g_m/g_{ds}, and (b) f_T and I_D/W disagreements.

Table III Changes in ring oscillator delay after the calibrations

Gate Length [μm]	0.18	0.28	0.36	0.44
After Subthreshold Cal. [%]	+0.00	+0.05	+0.04	+0.00
After g_m/g_{ds} Cal. [%]	+0.29	+0.23	+0.26	+0.25
After f_T and I_D/W Cal. [%]	+6.38	+7.56	+8.01	+8.31

Acknowledgements

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