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Write Speed Evaluation of Reconfigurable Spin Logic Block with SPRAM for 3D-Stacked Reconfigurable Spin Processor

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1. Introduction

A programmable device like reconfigurable logic LSIs was widely used for various signal processing applications. However, these systems have problems related to power dissipation when using SRAM as a configuration memory. Although power gating is one of the standby power reduction techniques, it's difficult to use for SRAM based reconfigurable logic LSI. To realize low power and true dynamic reconfigurable system, we have proposed a 3D (three-dimensional) stacked reconfigurable spin processor which used SPRAM (SPin-transfer torque RAM) as the configuration memory instead of SRAM and other non-volatile memories such as flash memory and FeRAM [1]. The proposed 3D-stacked reconfigurable spin processor consists of spin memory (SPRAM) layer, reconfigurable logic block array layer, and processing array layer. These layers are vertically connected with high density Through-Si Vias (TSVs). In the proposed reconfigurable spin processor, both configuration data and state data are stored in the SPRAM. Therefore, circuit configuration changes during execution of signal processing. In this paper, we describe write speed evaluation of reconfigurable spin logic block with SPRAM.

2. Circuit design and SPRAM cell evaluation

Figure 1 shows the block diagram of reconfigurable spin logic block which is a fundamental component of the reconfigurable spin processor. This logic block is composed of four-input LUT (Look-Up Table), output flip-flop, and 16-bit SPRAM cells and peripheral circuits. The four-input LUT consists of 16 inputs MUX and 16-bit SRAM. The SPRAM cell has a cell transistor and a MTJ (Magnetic Tunnel Junction). We measured SPRAM cell characteristics before detailed evaluation of write operation. Figure 2 shows V-I and V-R characteristics of SPRAM cell, where we defined a current flow from BLT to BLB as forward current. The MTJ resistances are 1.14 kΩ and 2.62 kΩ for R_P (Parallel) and R_{AP} (Anti-Parallel), respectively. The switching currents are 165 μA and -353 μA for forward current (R_{AP} to R_P) and reverse current (R_P to R_{AP}), respectively. Figure 3 shows simulated V-I and V-R characteristics with MTJ SPICE model. The simulation results were almost identical to experimental results. The write circuit for SPRAM is illustrated in Fig. 4. The write circuit consists of write drivers for the SPRAM and a control logic circuit. The write drivers are controlled by the select terminal of "RW" and "WBEX". The RW selects read or write operation and the WBEX selects the write data from SRAM (terminal of "WBD") or external (terminal of "EXD"). To verify the write circuit operation, SPICE simulation was performed as shown in Fig. 5. The supply voltage is 1.0 V. The upper is MTJ current, the middle is MTJ resistance, and the lower is control signal of "WORD". When the WORD became high, the MTJ current increased and the MTJ resistance changed, indicating a proper circuit function. The write speed of R_P and R_{AP} were 5.24 ns and 13.8 ns, respectively.

3. Write speed evaluation

To evaluate the circuit properties of the reconfigurable spin logic block, logic circuits were fabricated with a standard one-poly five-metal 90 nm CMOS technology and MTJ was fabricated on the logic circuits successively. The MTJ consists of CoFeB for ferromagnetic layer and MgO for tunneling barrier layer. The size of MTJ is 250 × 530 nm^2 (MTJ-1) and 250 × 510 nm^2 (MTJ-2). The write circuit and SPRAM are shown in Fig. 4. To obtain sufficient write-current, the write circuit contains boot-strap function. Using boot-strap function, the supply voltage of the circuit is boosted to 1.8 V during write operation. Figure 6 shows the measured signals of EXD, WORD, and BLT during the write operation. The EXD was set to high for execution of R_P write operation. When the WORD rose, the BLT fell step by step. This means that MTJ switching had occurred successfully. In this study, the write time is defined as minimum pulse width of the WORD signal which is enough time to change the MTJ resistance. As for Fig. 6, the WORD pulse width more than 60 ns was used to show the switching phenomena obviously. From the write speed measurements, the fastest switching speed of 5 ns was achieved in our circuit, showing the possibility of true dynamic reconfiguration.

Figure 7 summarized R_P write time, MTJ switching current, and MTJ resistance for 7 chips. There is a positive correlation between the MTJ switching current and write time. This is because that the magnetization switching tends

to occur for the MTJ with low switching current [2]. As results, the average R_P write time of 7.5 ns was obtained in the reconfigurable spin logic block.

4. Conclusion

The SPRAM cell operation and write speed evaluation of the reconfigurable spin logic block with SPRAM were presented. The test chip was fabricated in a standard one-poly five-metal 90 nm CMOS technology and successive MTJ formation. The fastest switching speed of 5 ns was achieved in the circuit. The SPICE simulation with a MTJ model was performed for the proposed circuit and verified circuit operation. These results indicated the possibility of true dynamic reconfiguration for 3D-stacked reconfigurable spin processor.

Acknowledgement

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References

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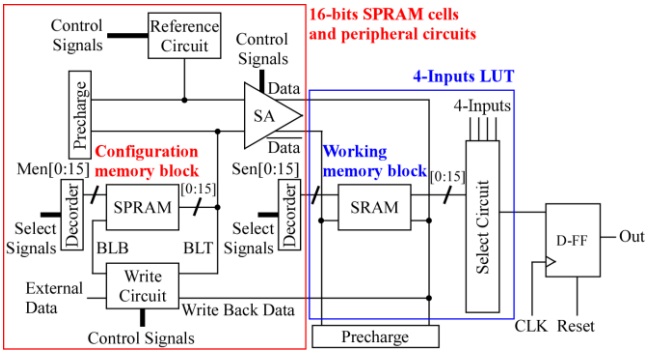
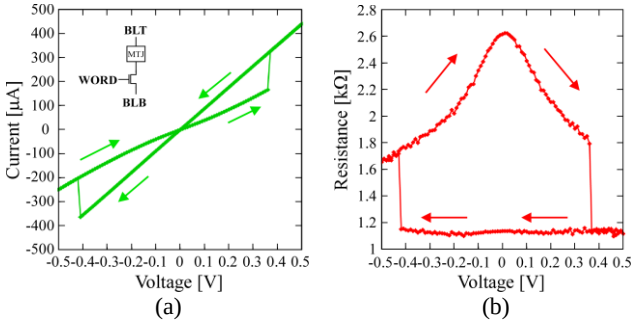
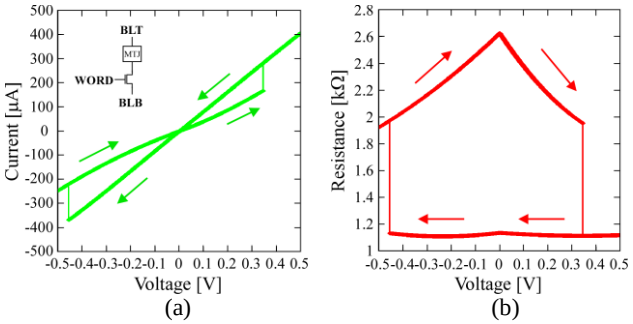


Fig. 1. Diagram of reconfigurable spin logic block.



(a) (b)

Fig. 2. Measured characteristics of SPRAM cell:
(a) V-I characteristics; (b) V-R characteristics.



(a) (b)

Fig. 3. Simulated characteristics of SPRAM cell:
(a) V-I characteristics; (b) V-R characteristics.

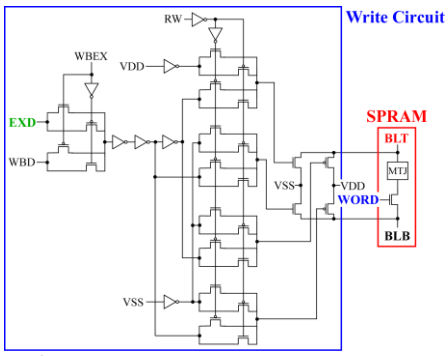
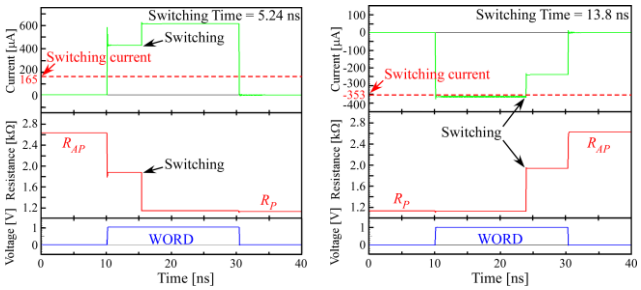


Fig. 4. SPRAM write circuit.



(a) (b)

Fig. 5. SPICE simulation results of the SPRAM write circuit:
(a) R_P write operation; (b) R_{AP} write operation.

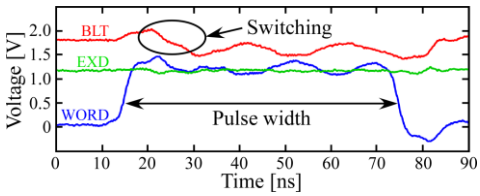
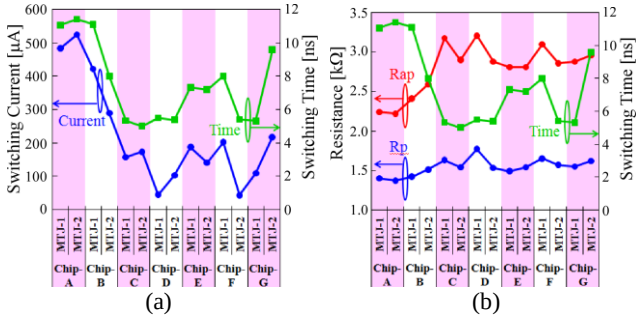


Fig. 6. Measured waveforms for R_P write operation.



(a) (b)

Fig. 7. Average values for 7 chips (16 SPRAMs per chip):
(a) Switching current and switching time;
(b) Resistance of SPRAM and switching time.