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Nonvolatile Low Power 16-bit/32-bit MTJ Based Binary Counter and its Scaling

Shuta Togashi[1,2], Takashi Ohsawa[2], and Tetsuo Endoh[1,2]

[1]Center for Interdisciplinary Research, Tohoku University, 6-3 Aramaki Aza-Aoba, Aoba-ku, Sendai 980-8578, Japan
Phone: +81-22-795-4401 E-mail: endoh@riec.tohoku.ac.jp
[2]Center for Spintronics Integrated Systems, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan

1. Introduction

Magnetic tunnel junction (MTJ) is expected to be used in logic LSIs to reduce power by power-gating (PG) inactive circuits with latched data stored in the nonvolatile devices. The designs can realize low-power electronic systems without performance sacrifice [1]. However, a family of logic circuits that have advantages in making them nonvolatile are not widely known.

In this paper, we propose a novel nonvolatile 16-bit/32-bit MTJ based binary counter with PG scheme suitable for MTJ that is constructed by the nonvolatile binary counter unit [2]. The power of the unit and the multi-bit counters are estimated by our developed NS-SPICE_MTJ [3] that can seamlessly simulate the CMOS/MTJ hybrid circuits. It is shown that the proposed 16-bit/32-bit binary counter achieves lower power than the conventional CMOS binary counter. Furthermore, its scalability is made clear till 16nm CMOS technology node.

2. Nonvolatile Binary Counter Unit

The conventional CMOS counter unit is shown in Fig. 1, where two latches operate interchangeably at a frequency so that it generates a clock whose frequency is doubled [4]. The proposed nonvolatile counter unit is shown in Fig. 2, where only one nonvolatile latch realizes the same function in addition to saving the latched data into the MTJs during power down [2]. Fig. 3 illustrates its operating waveforms. The decreased number of devices itself contributes to the power reduction. On top of that, the power supplied to the unit (Vpg) can be shut down by raising $/\phi_n$ when it is not working, further reducing the power due to the subthreshold leakage. The PG period is indicated by PG in Fig. 3.

Fig. 4 shows the comparison between the operating power of the proposed counter unit and that of the conventional one, both of which are simulated by NS-SPICE for 45nm and 16nm nodes. The parameters of the MOSFETs and the MTJ we assumed in the simulations are summarized in Table I. In the low frequency region, both powers are independent of the frequency, indicating that they are dominated by the subthreshold leak currents. The power of the proposed unit is about 60% smaller than the conventional one in the region, because the former is power-gated by a long channel PFET with a high threshold voltage. As the frequency increases, the both powers increase due to the increase of the dynamic power for charging the capacitors of the internal nodes. For the case of the proposed unit, the switching power of the MTJs is consumed in addition to the dynamic power in the higher frequency region, making the power curve start to bend up at a lower frequency than the conventional one. The cross points are observed to be at 2.5KHz and 220KHz for 45nm and 16nm, respectively. Fig. 5 shows the trend of the cross point frequencies from 45nm node to 16nm node. The frequency region where the proposed counter consumes less power than the conventional one expands to a higher frequency area as the devices are scaled down.

3. Nonvolatile 16-bit/32-bit Binary Counter

We first examine a 16-bit nonvolatile counter as shown in Fig. 6. The operating frequency for the n-th bit, is $f_n=f_0/2^n$, where f_0 is the frequency of the 0-th bit or LSB. The counter unit for more significant bit is more effectively power-gated, because the duty cycle of active operation for the unit is smaller for more significant bits.

Fig. 7 shows the power comparison between the conventional 16-bit counter and the nonvolatile 16-bit counter with the proposed unit for 45nm and 16nm. Though they exhibit the same tendency as Fig. 4, the cross point frequencies are 23KHz and 1.9MHz respectively for 45nm and 16nm, which are larger than those for the counter unit, indicating the counter is more effectively power-gated for the units of more significant bits. Fig. 8 is the same kind of graphs as Fig. 7 for the 32-bit counter. Fig. 9 shows the trend of the cross point frequencies for the 16-bit and the 32-bit counters from 45nm to 16nm. Since the subthreshold leak increases as MOSFETs are scaled down, the PG becomes more effective in the future. In 16nm node, the proposed 32-bit nonvolatile counter consumes less power than the conventional one even at 4MHz.

There is a way to lower the counter power further as shown in Fig. 10. In this counter design, less significant bits where larger overhead of PG is expected are counted by the conventional volatile units and more significant bits where PG is applied more effectively are counted by the proposed nonvolatile units. Fig. 11 shows the power comparison between this hybrid type of 32-bit counter and the conventional one in 16nm node. It is observed that by the above novel PG scheme suitable for MTJ, this hybrid counter consumes less power than the conventional one up to 1GHz. Although this counter is a volatile one, it achieves a low power counter in a wide range of frequency.

4. Conclusion

We propose a novel nonvolatile 16-bit/32-bit MTJ based binary counter with PG scheme suitable for MTJ. The proposed nonvolatile 32-bit counter achieves lower power up to 49KHz and 4MHz in case of 45nm node and 16nm node, respectively, in comparison with the conventional CMOS counter. Moreover, it is shown that the proposed hybrid multi-bit counter achieves lower power up to 1GHz than the conventional CMOS counter. From all, the scalability of the proposed MTJ based multi-bit counter is made clear from view point of suppressing power.

Acknowledgements

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References

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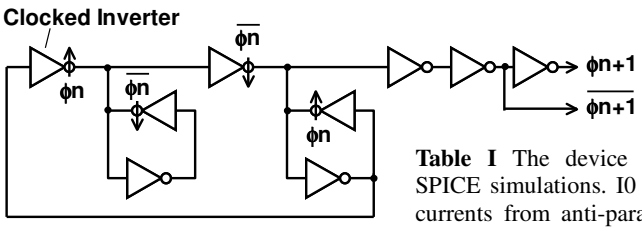

Fig. 1 The conventional counter unit.

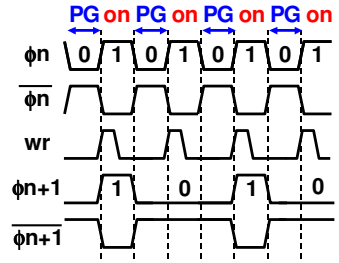

Fig. 3 The operating waveforms of the proposed counter.

Table I The device parameters used in the SPICE simulations. I0 and I1 are the switching currents from anti-parallel (AP) to parallel (P) and from P to AP, respectively. R0 and R1 are the resistances of P and AP, respectively.

Technology node		45nm	32nm	22nm	16nm
Vdd [V]		1	0.9	0.8	0.7
Tr.	Wn [nm]	270	189	135	91.8
	Wp [nm]	420	294	210	142.8
	L [nm]	50	35	25	17
MTJ	I0 [μA]	50	25	12.5	6.25
	I1 [μA]	100	50	25	12.5
	R0 [kΩ]	4	8	16	32
	R1 [kΩ]	8	16	32	64

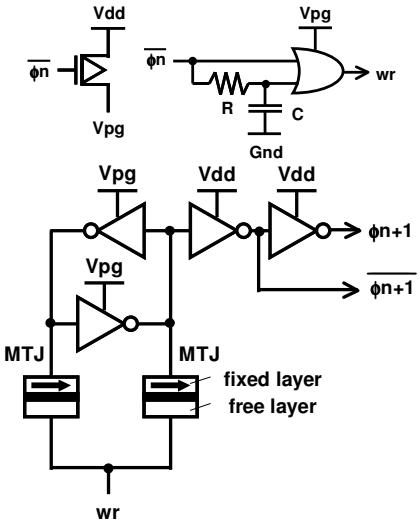

Fig. 2 The proposed nonvolatile counter unit.

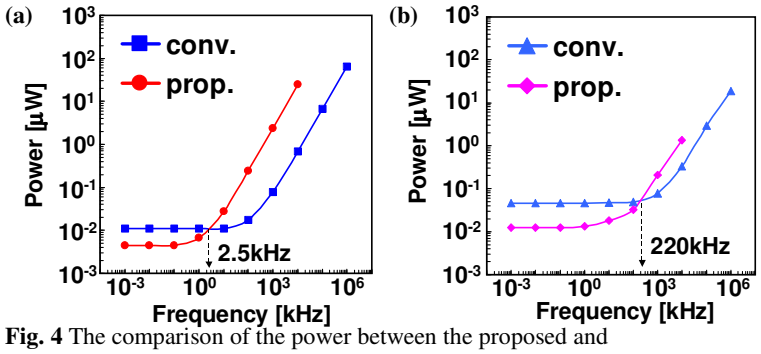

Fig. 4 The comparison of the power between the proposed and the conventional counter units for (a) 45nm node and (b) 16nm node.

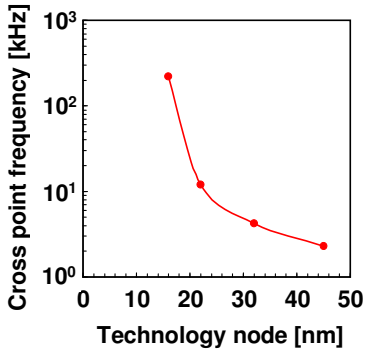

Fig. 5 The trend of the cross point frequencies for the counter units from 45nm node to 16nm node.

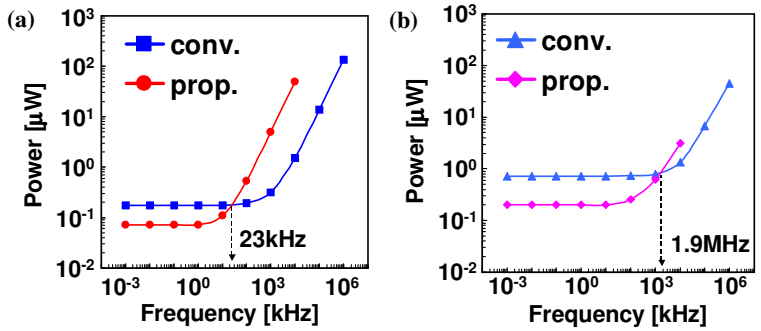

Fig. 7. The comparison of the power of the 16-bit counter using the proposed units and that using the conventional units for (a) 45nm node and (b) 16nm node.

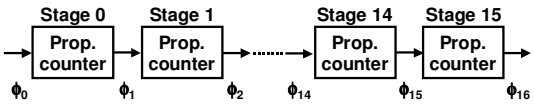

Fig. 6 16-bit nonvolatile counter.

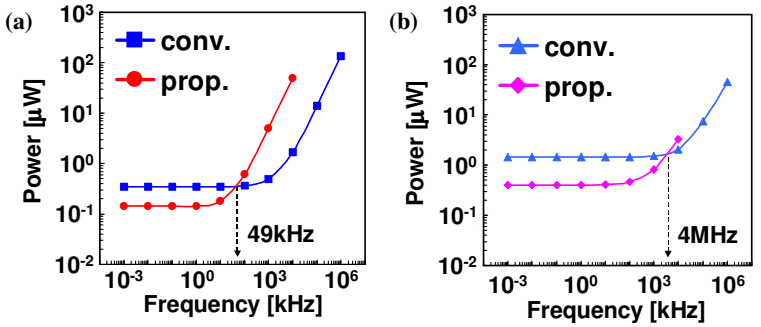

Fig. 8 The comparison of the power of the 32-bit counter using the proposed units and that using the conventional units for (a) 45nm node and (b) 16nm node.

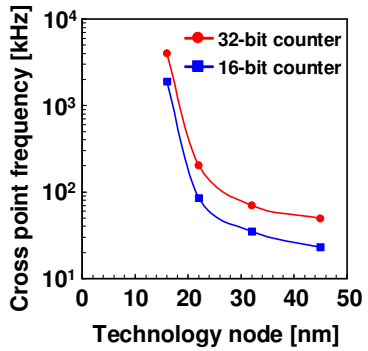

Fig. 9 The trend of the cross point frequencies for the 16-bit and the 32-bit counters from 45nm node to 16nm node.

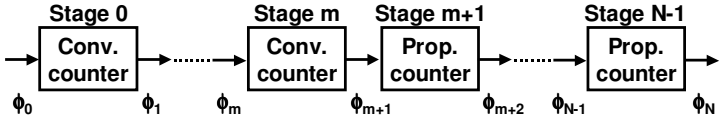

Fig. 10 N-bit hybrid counter design using both the conventional volatile and the proposed nonvolatile counter units.

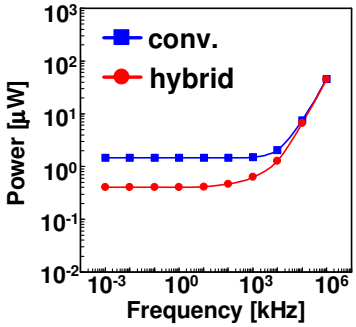

Fig. 11 The power comparison of the 32-bit counters between the conventional and the hybrid proposed.