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Evaluation of Reconfigurable Processor Test Chip for Dependable 3D Stacked Multicore Processor

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1. Introduction

The performance of microprocessor has been significantly improved by increasing the transistor performance. However the improvement of microprocessor performance based on the increase of transistor performance has resulted in the increase of power consumption. Then parallel processing using multicore processors has been introduced to suppress the increase of power consumption with increasing the microprocessor performance. However both chip area and total interconnection length significantly increase as the number of microprocessor cores increases and consequently the power consumption increases. Furthermore such multicore processor with a large chip size and long interconnection length gives rise to the reduction of production yield and dependability. To overcome these problems in multicore microprocessors, it is indispensable to cut a large chip into several smaller chips and vertically stack and electrically connect them by the through silicon vias (TSVs). Then we have proposed a 3D stacked multicore microprocessor with a smaller form factor, reduced power consumption and increased dependability as shown in Fig.1 [1]. This 3D multicore microprocessor consists of several processor tiers, several memory tiers and built-in self-test (BIST)/repair tiers. These tiers are connected by high density of TSVs [2]. In our 3D multicore microprocessor, realtime self-test and failover operation are performed using BIST/repair tiers. When failures occurred, failed module is replaced by redundant module in BIST/repair tier and tasks on replaced module are allocated to active modules.

In this paper, we have evaluated the fundamental failover operation in a test chip for such 3D microprocessor.

2. Failover Operation in 3D Stacked Microprocessor

The replacement by redundant module and task migration are essential to implement the failover operation in 3D multicore microprocessor. Then we designed a test chip for such 3D multicore microprocessor. This test chip contains four simple processors with reconfigurable SIMD/MIMD function and I/O switches to select one of four tiers. Therefore four test chips can be stacked to evaluate the failover operation as shown in Fig.2. This stacked chip consists of one redundant tier and three active tiers. Fig. 3 shows operations of the stacked reconfigurable processors which are constructed by four test chips. In normal operation, active tiers process provided tasks and redundant tier is in a cold standby state. When a failure is detected during real-time self-test, failed tier is disabled and then redundant tier becomes in active state. The tasks are processed using all active tiers except a failed tier. Thus, failover operation is performed by replacing module and switching of routing paths for tasks.

3. Evaluation Results of Failover Operation

The reconfigurable processor test chip was fabricated by CMOS 130nm technology. Fig. 4 shows the microphotograph of the reconfigurable processor test chip. The chip area was 5.0mm x 5.0mm. The reconfigurable processor test chip operated at 40MHz. This reconfigurable processor test chip can process a gray scale image with 32 x 32 pixels x 4. The image processing function in this reconfigurable processor test chip depends on configuration data in the chip. In order to evaluate basic failover function in a 3D stacked microprocessor, packaged test chips are vertically stacked as shown in Fig. 5. Image processing function extending over every two pairs of stacked chips, tier 1 and tier 2, tier 2 and tier 3, and tier 3 and tier 4, was examined to evaluate the failover function in four stacked test chips since it was difficult to vertically stack four packed test chips. We evaluated the task migration function to repair failed modules through vertical interconnection which is the essential feature in a dependable 3D microprocessor. Fig. 6 shows output images processed by reconfigurable microprocessor test chips in each tier, when four edge detection tasks are provided to the respective tiers of stacked test chips. Four source images of Barbara, cameraman, airplane and Lenna are applied to the respective tiers for the edge detection. First, Barbara, cameraman, airplane and Lenna are processed by tier 1, tier 2, tier 3 and tier 4, respectively. Then routing paths for tasks are changed by input switch and output switch assuming that the tier 1 failed as shown in Fig.3 (b). Images after the edge detection in tier 2, tier 3 and tier 4 before the task migration are shown in Fig.6 (b) whereas those in the same tiers after the task migration are shown in Fig.6 (c). It is obvious that images of tier 2, tier 3 and tier 4 changed from cameraman, airplane and Lenna before the task migration to Barbara, cameraman and airplane after the task migration. Thus it was confirmed using test chips that the failover operation by the task migration is successfully performed in a 3D stacked microprocessor.

4. Conclusions

We designed a reconfigurable microprocessor test chip to evaluate fundamental function of dependable 3D multicore microprocessor. Packaged test chips are vertically stacked and image processing function extending over every two pairs of stacked chips was examined. It was confirmed using these test chips that the failover operation by the task migration is successfully performed in a 3D stacked microprocessor.

Acknowledgements

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References

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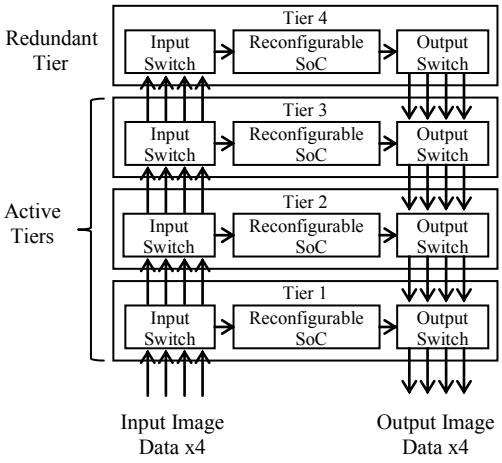

Fig. 2 Configuration of stacked microprocessor test chips.

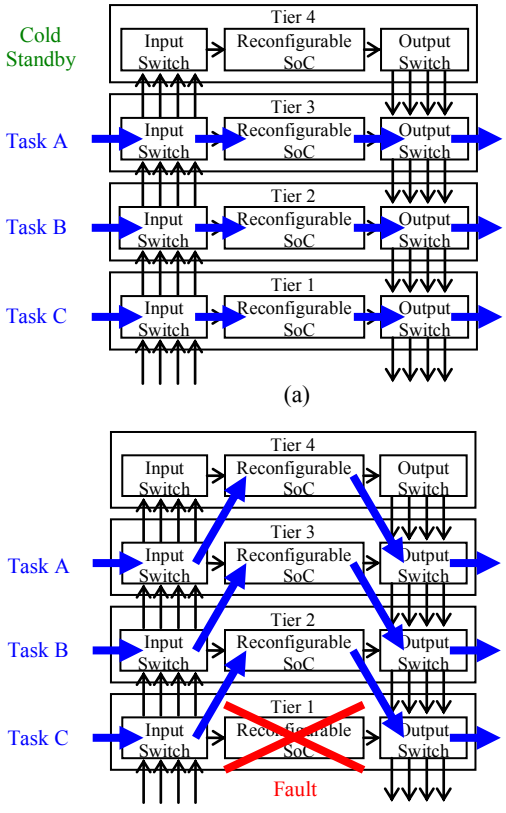

Fig. 3 Normal operation (a) and failover operation after routing paths for tasks are switched (b) of stacked reconfigurable processor test chips

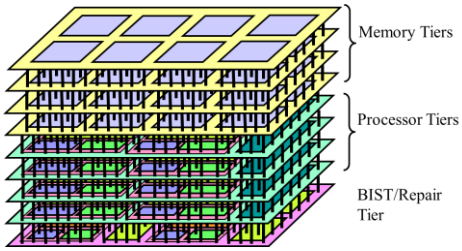

Fig.1 Configuration of dependable 3D multicore microprocessor.

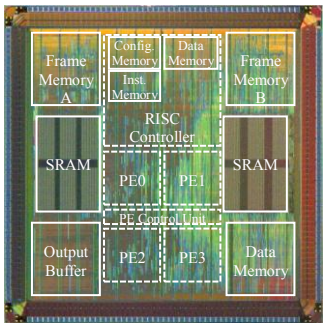

Fig. 4 Chip microphotograph of microprocessor test chip.

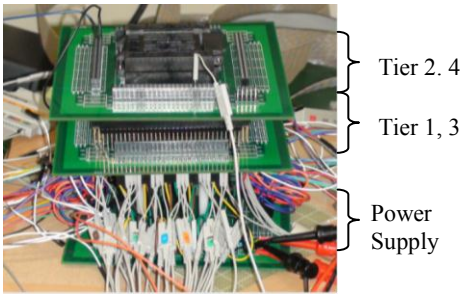

Fig. 5 Evaluation of failover function using stacked microprocessor test chips in package level.

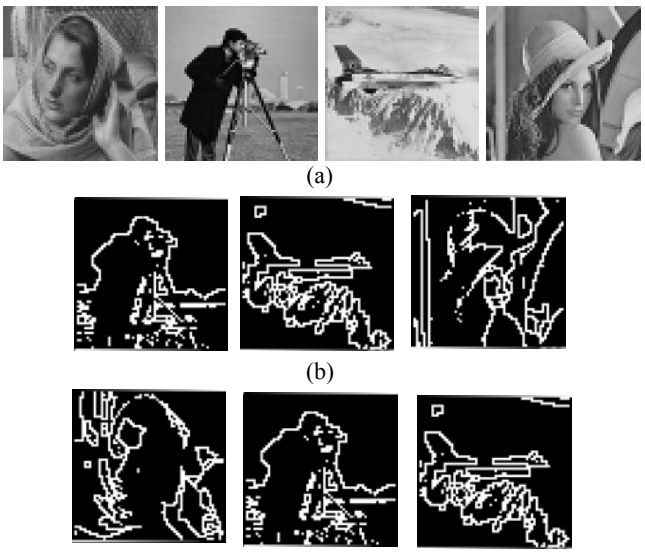

Fig. 6 Source Images (Barbara, cameraman, airplane and Lenna) (a). Cameraman, airplane and Lenna processed by tier 2, tier 3 and tier 4, respectively (b). After routing paths for tasks are changed, Barbara, cameraman and airplane processed by tier 2, tier 3 and tier 4, respectively (c).