The Integrated a-Si Gate Driver Circuit using Voltage Controlled Capacitance Modeling for HDTV/XGA

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1. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors(TFTs) are the most widely used switching devices in active matrix liquid crystal displays. AMLCDs have been applied to many information tools such as personal computers, PDAs, and picture displays. In recent years, a-Si TFT gate driver integration has become indispensible in TFT-LCD business because of the reduction in fabrication cost by eliminating external gate driver ICs and the advantage in realizing slim displays.

An a-Si:H integrated gate driver for TFT-LCD was operated using bootstrapping technology owing to small mobility in the range of 0.3 to $0.6 \text{ cm}^2 \text{V}^{-1} \text{S}^{-1}$. In design step of an a-Si:H integrated gate driver, it's necessary to define some design factors that can affect bootstrapping characteristic. This is related with capacitance characteristics of integrated transistors. So, we focused on TFT devices, modeling, and the a-Si:H integrated gate driver circuit using the voltage controlled capacitance modeling method. From understanding the relation between capacitance characteristics of a-Si:H integrated transistors and gate output signal, it's possible to design an a-Si:H integrated gate driver for high resolution and driving frequency of TFT-LCD

2. General Instructions

An a-Si:H integrated gate driver circuit for TFT-LCD is described, especially focusing on the charging time and discharging time for HDTV/XGA. These are imperative for robust circuit design and the quality of picture. In design step of an a-Si:H integrated gate driver, it's necessary to define gate falling time exactly.

In this paper, we investigated the capacitance characteristics and modeling using the new extracted method. The relation between capacitance characteristics of a-Si:H integrated transistors and gate output signal is analyzed using UTMOST and SMARTSPICE simulator. The accuracy of the simulated gate output signal using voltage controlled capacitance modeling is verified with measured data.

Figure 1 illustrates the equivalent circuit models of the conventional and the proposed structures. The volt-age-controlled capacitance (VCCAP) is used for compensating the capacitance characteristics of inverted staggered a-Si:H TFT.[1]-[2]



Fig.1. Equivalent circuits of (a) the conventional TFT model using geometric capacitance per unit area and (b) the proposed TFT model using voltage controlled capacitance.

Figure 2 shows the back channel etched structure, the measured and simulated C-V characteristics in both the electron accumulation and depletion range of the gate voltage of fabricated a-Si:H TFT.



Fig.2. (a) Cross sectional view and (b) Measured and Simulated C-V Characteristics of an inverted stagger a-Si:H TFT at 27° C and 50kHz

The gate drivers essentially drive all the rows on the backplane one at a time for a frame time.[3] Each stage consists of shift register cells and buffer transistors.(T6 and T7) Figure 3 shows T6 was operated for pulling up and down the output logic. T7 acts to hold the output to a logic low. The capacitance characteristics of all transistors are very important design issue. Because these affect Q node and the gate output due to bootstrap effect.



Fig.3. Circuit showing the shift register cell in the gate driver (a) Conventional shift register (b) Proposed shift register.

Figure 4-(a) shows rising and falling time of a-Si:H integrated gate driver output signal were measured with Oscilloscope DPO7054 Tektronix product. And Figure 4-(b) shows simulation results of the proposed and conventional gate driver circuits. Node 'Q' experiences an increase in the voltage due to bootstrap effect. The proposed gate driver has been increased 11.6% (charging Time) and 28% (discharging time) for conventional structure. The measured and simulated output results are summarized in Table 1





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(b)

Fig.4 Measured and simulated results of the proposed and conventional gate driver circuits. (a) Measured results showing rising and falling time. (b) Comparison of charging and discharging time between the proposed and conventional gate driver circuit

Table1 Comparing a predicting rising and falling time with measure results

Items		Rising Time	Falling Time
Meas.		2.360u	2.040us
Sim.	Proposed	2.249us(95.3%)	2.212us (92%)
	Conventional	2.014us(85.3%)	1.726us (85%)

3. Conclusions

For applying a-Si:H integrated gate drive to a large size and high frequency LCD TV, it's important to understand the property of integrated gate driver. With the reason, it's necessary to develop a method or tool to predict the gate output signal exactly. In out study, the a-Si:H gate driver using voltage controlled capacitance modeling increased the accuracy of rising (95.3 %) and falling time(92%).

4. Acknowledgements

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