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Current Compensation Circuit for Precise Nano-Ampere Current Reference

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1. Introduction

We developed a current compensation circuit for precise nano-ampere current reference. In recent studies, a nano-ampere current reference circuit was presented [1]-[3]. However, the generated current increased with temperature. A compensation technique for the current was also proposed in [1]. However, because the circuit used complementary current sources, the chip area and power dissipation increased significantly. Moreover, because the accuracy of the compensated current was limited by temperature dependences of the carrier mobilities, the compensation was insufficient for high accuracy. To solve the problems, we developed the current compensation circuit. Details of the circuit operations are as follows.

2. Circuit Configuration

Figure 1 shows the block diagram of our proposed compensation circuit. The circuit consists of a clock reference circuit, a nano-ampere current reference [1], a current add/subtractor control circuit, a current-to-voltage converter (IVC), a voltage monitor circuit (VMC), and a counter circuit. We use crystal oscillator for clock generation. The current reference circuit generates a nano-ampere order current I_n. As mentioned above, the I_n increases with temperature [1]. To compensate the temperature dependence of I_n, first, the IVC accepts the generated current I_n and generates a voltage V_C. The V_C is monitored by reference voltages of V_{REF1} and V_{REF2} in the VMC. We set the reference voltages such that V_{REF1} is higher than V_{REF2}. When V_C is higher than V_{REF1}, we can find that the current is higher than desired current. On the other hand, when V_C is lower than V_{REF2}, we can find that the current is lower than desired current. The VMC generates a digital signal according to the voltage level of V_C. The counter circuit stores the digitized information and control the current add/subtractor control circuit until the output current I_{REF} converges within desired current level.

Figure 2 shows our proposed circuit. The details of the circuit and circuit operation are as follows.

1. The current add/subtractor circuit is composed of current mirror circuit and switch transistors. The current mirror circuit generates weighted-current using smaller sized transistor than diode-connected transistors in the current reference circuit. The switch transistors accept digital signals from the counter, and the weighted-current is added or subtracted from I_n. The resultant current I_{REF} is applied to the IVC.
2. The IVC consists of a capacitor and switches driven by clock pulses (ϕ_1 and ϕ_2: ϕ_2 is a delayed pulse of ϕ_1). The current I_{REF} generates a ramp voltage V_C on the capacitor when ϕ_1 is high. The V_C is monitored by the VMC. Note that, because ϕ_2 is just a delayed pulse of ϕ_1, overlapping period between ϕ_2 and ϕ_1 exists. However, because the current level is nano-ampere order, power overhead is significantly small.
3. The VMC consists of two window comparators and a NAND gate. When V_C is higher than V_{REF1}, comparator CMP1 outputs low signal. The negative edge counter stores the information (DD*i*) and the current add/subtractor control circuit generates a corrected I_{REF}. On the other hand, when current I_{REF} is lower than target level, V_C is also lower than V_{REF2}. However, because comparator CMP2 keeps outputting high logic in this case, CMP2 cannot detect the low level of the current. To solve this problem, timing detection circuit consisting of NAND gate with clock ϕ_1 and $\overline{\phi}_2$ is used. In our design, both ϕ_1 and $\overline{\phi}_2$ have high logic at the evaluation time. So, the NAND gate can generate a negative edge signal at the period. The negative edge counter stores the information (DU*i*) and the current add/subtractor control circuit generates a corrected I_{REF}.

3. Results

We evaluated the proposed circuit using 0.35-μm standard CMOS process. In this evaluation, clock frequency and capacitance were set to 2.5 kHz and 10 pF, respectively. The reference voltages V_{REF1} and V_{REF2} were set to 750 mV and 700 mV, respectively.

Figure 3 shows the waveforms of V_C at the condition where initial current levels are higher (left) and lower (right) than desired current level. From the left, when V_C is higher than V_{REF1}, current level was reduced by each clock cycle. In a similar way, when V_C is lower than V_{REF2}, current level was increased by each clock cycle. Figure 4 shows the histograms of the output current. Monte Carlo simulations considering D2D and WID variation were performed with and without compensation circuit. Without compensation circuit, the distribution was broad in the range of 30 nA to 47 nA. The coefficient of variation CV (σ/μ, σ: standard deviation and μ: mean value) was 6.93%. With compensation circuit, CV can be made small and was 2.85%. Figure 5 shows the results of current I_{REF} as a function of temperature. The temperature dependence was derived from transient response by changing the temperature from –20 to 100°C with 2°C steps. Without compensation circuit, the output current I_{REF} increased with temperature. On the other hand, with compensation circuit, temperature dependence can be improved significantly. The temperature

variation can be improved from 13.2 nA to 1.8 nA by using our circuit. Table 1 summarizes circuit performances.

Our proposed circuit can compensate for the current variation not only due to temperature change but also due to process variations. Thus our proposed circuit is useful as a current reference circuit for a micro-power LSIs.

References

[1] T. Hirose *et al.*, *The 36th ESSCIRC*, pp.114-117, 2010.

[2] K. Ueno *et al.*, IEEE JSSC, pp. 2047-2053, 2007.

[3] Y. Osaki *et al.*, JJAP, pp. 04DE08-1 - 04DE08-6, 2011.

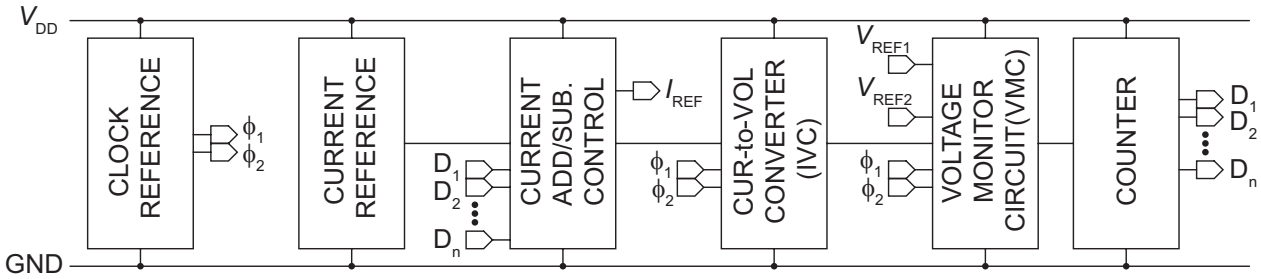

Fig.1 Block diagram of our current compensation circuit.

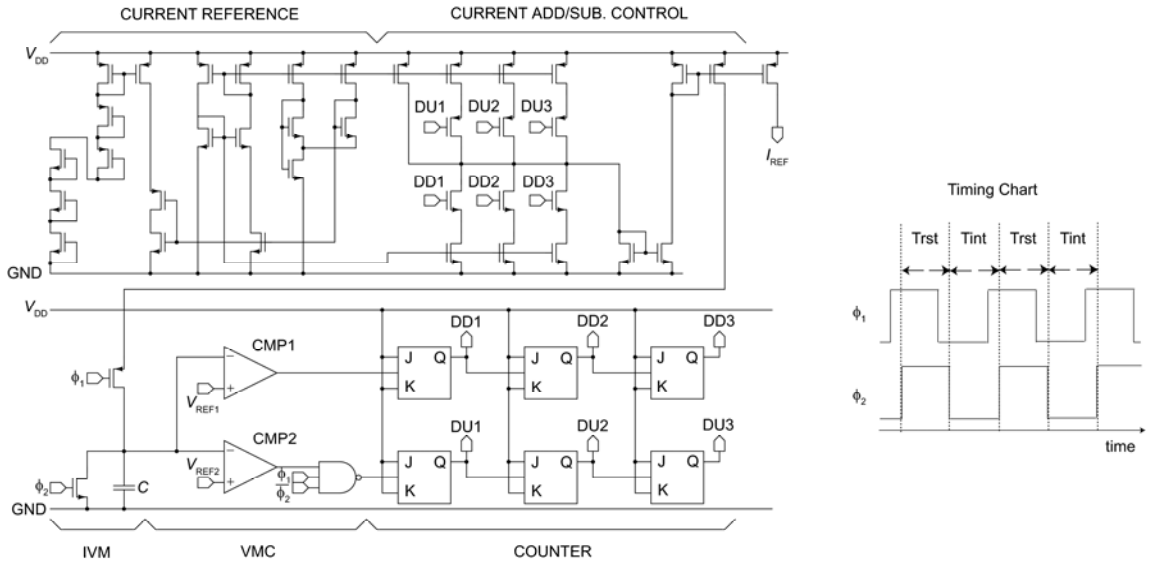

Fig.2 Proposed current compensation circuit and its timing chart. Tint: monitoring period, Trst: reset period.

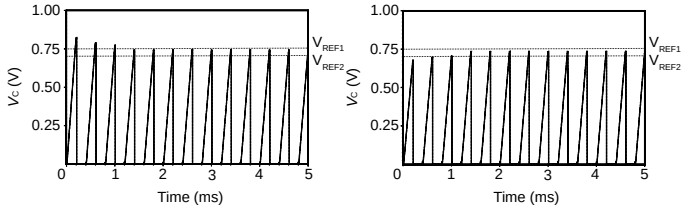

Fig.3 Waveforms of V_C when initial current levels are higher (left) and lower (right) than target current level.

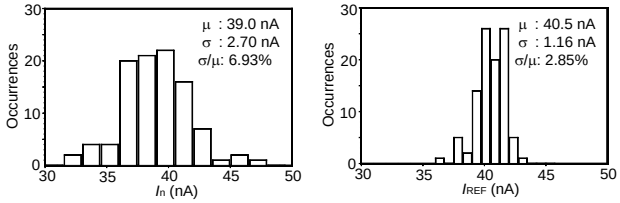

Fig.4 Histogram of the current without (left) and with (right) compensation circuit.

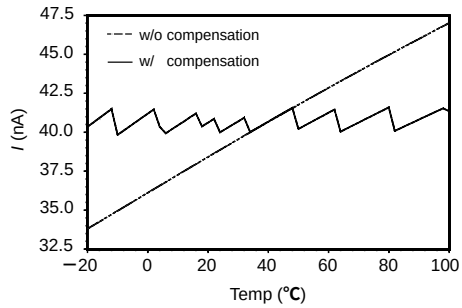

Fig.5 Output current I_{REF} as a function of temperature

Table 1 Performance Comparison

	This work	[1]	[2]	[3]
Technology	0.35-μm	0.35-μm	0.35-μm	0.35-μm
Temp.(°C)	-20 – 100	-20 – 80	-20 – 80	-20 – 100
I_{REF} (nA)	40.5	10	36	94.9
ΔI_{REF} (nA)	1.8	7.2	8.0	NA
TC (ppm/°C)	370	1190	2222	523
Process variation CV	2.85%	14.1%	NA	NA