# Hot Carrier Effect on RF Characteristics of High-k/Metal Gate SiGe Channel pMOSFETs

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## 1. INTRODUCTION

Strain engineering and new channel materials such as germanium, strained silicon-germanium, and III-V compounds have been investigated to enhance the performance of CMOS devices [1]. Especially, the SiGe material has been widely used because of its higher mobility than Si and good process compatibility with Si [2]. The reliability for the SiGe material has been intensively studied in DC region, but the study of the reliability in radio frequency (RF) is needed because RF applicability of the SiGe devices increases due to its higher mobility. In particular, the SiGe pMOSFETs increases the impact ionization at the drain edge region because of their narrow band gap energy compared with Si pMOSFETs [3]. Therefore, hot carrier injection (HCI) should be studied to provide deeper understanding for RF reliability of SiGe devices. In this paper, we report the effect of HCI on RF performance of SiGe pMOSFETs based on the analysis of RF small-signal parameters. Additionally, the role of Si capping layer on SiGe channel in hot carrier instability is also investigated, comparing with Si pMOSFETs as a control device.

#### 2. EXPERIMENTS

The thickness of epitaxial SiGe layers and the concentration of Ge were optimized to 5 nm and 25 %, respectively. A 3 nm Si capping layer was deposited to encapsulate the SiGe channel, as shown in Fig. 1. A 3 nm HfO<sub>2</sub> layer was deposited by atomic layer deposition (ALD) on a 1 nm interfacial layer (IL). TiN was deposited by ALD as the gate electrode. Si pMOSFETs as a control devices were also fabricated as 2 fingers devices with a finger width of 20 µm and a gate length of 180 nm. Detailed split conditions are shown in Table I [4]. The stress condition was chosen to apply the same vertical and lateral field in both SiGe pMOSFETs and Si pMOSFETs, considering the effective gate length and EOT. The hot carrier stress was applied at  $V_G = V_D = -2.5$  V for Si pMOSFETs and  $V_G$  = -2.5 V,  $V_D$  = -2.3 V for SiGe pMOS-FETs. For RF characteristics, S-parameters were measured in the frequency range from 1 GHz to 20 GHz by using Anritsu 37397C vector network analyzer (VNA).

## **3. RESUTS AND DISCUSSION**

As shown in Fig. 2, the SiGe pMOSFETs showed higher I<sub>D</sub> and  $g_m/C_{inv}$  than Si pMOSFETs, which was attributed to the higher mobility. To extract the intrinsic RF small-signal parameters, the effect of the source/drain series resistance ( $R_{sd}$ ) should be removed. The  $R_{sd}$  and  $R_s$  was determined by extrapolating Re( $Z_{22}$ ) and Re( $Z_{12}$ ) at high gate voltages respectively as shown in Fig. 3 [5]. After the  $R_{sd}$  correction, the  $C_{gs}$  and  $C_{gd}$  were extracted from Y-parameters of intrinsic part of the device before and after the hot carrier stress. Both  $C_{gs}$  and  $C_{gd}$  decreased after the stress and increased slightly

after the relaxation as shown in Fig. 4. The degradation of  $C_{gs}$  (SiGe : 31 %, Si : 13 %) was higher than that of  $C_{gd}$  (SiGe : 4 %, Si : 2 %), which was attributed to the larger hole trapping to pre-existing defects of high-k layer at the source edge region [6]. The degradation of  $g_m$  in SiGe pMOSFETs (50 %) was higher than that of  $g_m$  in Si pMOSFETs (24 %) shown in Fig. 5.

In terms of RF performances, the  $C_{gg}$  ( $C_{gg} = C_{gs} + C_{gd}$ ) and transconductance ( $g_m$ ) are related with the current gain cutoff frequency ( $f_T$ ) which is expressed as

$$f_T \cong \frac{g_m}{2\pi (C_{gs} + C_{gd})} \tag{1}$$

Even though  $C_{gg}$  decreased,  $f_T$  decreased because of more severe degradation of  $g_m$ . Due to the higher degradation of  $g_m$ in SiGe pMOSFETs than that of  $g_m$  in Si pMOSFETs, the degradation of  $f_T$  in SiGe pMOSFETs (15 %) was more serious than that of  $f_T$  in Si pMOSFETs (8 %) after the stress (Fig. 5). Because the band gap of SiGe is smaller than that of Si, the probability of impact ionization in the SiGe channel increases. Therefore, the higher degradation of  $f_T$  in SiGe pMOSFETs was attributed to the higher degradation of  $g_m$ due to the new trap generation by injected hot hole into the IL.

Additionally, in terms of carrier injection, SiGe pMOS-FETs have longer distance for injection to the gate dielectric because the Si capping layer resulted in a deeper channel than Si pMOSFETs as shown in the Fig. 6. To analyze the role of Si capping layer in HCI, the stress condition ensuring the same impact ionization rate in the channel was used. As shown in Fig. 7, the stress condition could be determined by using the impact ionization ratio  $(I_b/I_s)$  as an index of the electrons generated by impact ionization. Under the stress, the degradation of  $f_T$  was similar in both devices shown in Fig. 8. Therefore, in terms of hot carrier-induced degradation, the role of Si capping layer is almost negligible.

#### 4. CONCLUSION

In terms of RF performance, the degradation of  $f_T$  in SiGe pMOSFETs was more severe than the Si pMOSFETs because the narrow band gap of SiGe channel resulted in more severe degradation of  $g_m$ . Under the stress condition ensuring the same impact ionization ratio in both devices, the Si capping layer on SiGe channel has not considerable effect on HCI.

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Fig. 1. Process flow and TEM image of device structure for SiGe/Si pMOSFETs with high-k/metal gate dielectric gate stack



Fig. 2. Comparison of DC characteristics of SiGe pMOSFETs and Si pMOSFETs

Si SiGe Si capping layer 0 Х EOT (nm) 1.1 1.1 High-k dielectric 3nm HfO<sub>2</sub> 3nm HfO<sub>2</sub>  $R_{sd}(\Omega)$ 30 35  $\mu_{eff}$  (cm<sup>2</sup>/V-sec) 43.1 68.4



Fig. 3. Extraction of  $R_d$  and  $R_s$  from the real part of Z-parameters



Fig. 4. The degradation of capacitance under the HCI (a) in SiGe pMOSFETs and (b) in Si pMOSFETs



Fig. 6. The band diagram of SiGe pMOS-FETs with Si capping layer



Fig. 7. The ratio of impact ionization  $(I_{Bulk}/I_{Source})$  versus drain voltage



Fig. 5. Comparison of variation of  $f_T$  and  $g_m$  between SiGe pMOSFETs and Si pMOSFETs under the HCI



Fig. 8. Comparison of variation of  $f_T$  and  $g_m$  under the stress ensuring the same impact ionization rate

# Table I. Split conditions of Si control and SiGe(Ge 25%) pMOSFETs