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2D Device Simulation of AlGaN/GaN HFET Current Collapse Caused by Deep Levels in GaN Buffer Layer

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1. INTRODUCTION

There are various mechanisms for AlGaN/GaN HFET drain current collapse, since drain current decreases by any process in which immovable negative charge emerges near the channel, such as gate edge surface [1]. One obvious another candidate is deep levels in GaN buffer layer which make the buffer layer semi-insulating. From the analysis on GaAs MESFET IC side-gating effects, it is clarified that semi-insulating layers act like n-type or p-type semiconductor layer in regard to electro-static potential profiles, that is electron-trap type as n-type and hole-trap type as p-type [2]. Electron-trap-type means that they exchange charges mainly with conduction band (electron) and hole-trap-types exchange with valence band (hole). The difference is almost determined by whether the trap energy level E_T is closer to E_V or E_C regardless of their capture cross sections. Deep traps in GaN buffer layer have investigated extensively and many levels E_C- E_T around 2 eV have been reported [3]. Since the bandgap of GaN is 3.4eV, these traps will be hole-traps. In this regard, we investigated the effect of the trap energy levels on the current collapse of AlGaN/GaN HFETs.

2. SIMULATION MODEL AND STRUCTURE

AlGaN/GaN HFET with channel length of 1μm and AlGaN thickness of 25nm (Fig.1) is assumed. Charges assumed are, 1×10^{13}cm^{-2} positive charge at AlGaN/GaN for the piezo-electric charge, 5×10^{16}cm^{-3} shallow acceptor and 1×10^{17}cm^{-3} deep donor in GaN buffer region. The capture cross sections of the trap for electrons and holes are both 1×10^{12}cm^{-2}. Two cases are assumed for the trap energy level, 0.4eV from the conduction band (electron-trap, ET) and 0.4eV from the valence band (hole-trap, HT). The emission time of electrons and holes are 1.2×10^{4}s and 1.8×10^{47}s for ET and 5.6×10^{47}s and 3.7×10^{3}s for HT, respectively. The case without traps and shallow levels in the buffer layer (NT) is also simulated. Synopsys Sentaurus was used for the simulation.

3. SIMULATION RESULTS

Id-Vd characteristics show good saturation characteristics both for ET and HT cases compared with NT case as shown Fig.2. Short-channel effects are suppressed by the deep traps terminating the electric flux from the drain region. The difference of the saturation current comes from the Fermi-pinning levels in the GaN buffer region.

Transient behaviors were analyzed where drain voltage was varied from steady state 10V to 0.1V in 1 ns and then, the biases were hold. First, the drain current abruptly decreases with the drain voltage. After the channel transit time of electrons, drain currents stay quasi-steady states [4]. The currents are determined by the trap charge distribution during the stress condition. Though we have not simulated, the current will reach the DC simulation values after sufficiently long time. The quasi-steady-state current and the DC steady state currents are compared (Table.1). The currents do not change for NT as expected, but the currents became smaller than their DC currents in ET and HT cases. In addition, the variations of the current are about 5 times larger for HT than ET.

Figure 3 shows the charge distribution at the stress condition at Vd=10V (left) and steady-state condition at Vd=0.1V (right). The final steady state charge distributions are similar, but at high Vd condition, they are largely different. For HT case, a negative charge region is formed beneath the drain, but for ET case both negative and positive charges appeared there. Due to the slow response of these deep trap charges, the charge distributions are kept in the quasi-steady state conditions.

Figure 4 compares the electrostatic potential distribution at the stress condition and the quasi-steady state, 10ns after the Vd change. Under the stress condition, potential for ET gradually vary from drain to source in the buffer region, but it abruptly vary under the drain region and almost flat in the buffer region under the channel. When the drain voltage is changed to 0.1V, potentials in ET case are all close to zero, but in HT case, negative voltage appears even though all the electrode potentials are close to 0V. This negative potential in the buffer causes the higher threshold voltage similar to the substrate bias effect of n-channel MOSFETs, and leads to the lower drain current.

4. CONCLUSIONS

Drain current reductions due to the trap in the GaN buffer layer is investigated by device simulation. Quasi-stationary drain current after the bias reduction is determined by the charge distribution formed in the stress conditions. The charge distribution profile under high drain bias is different depending on the trap properties in the buffer layer. From the simulation, it is estimated that hole-trap type deep levels cause severer collapse than those of electron-trap type.

Acknowledgements

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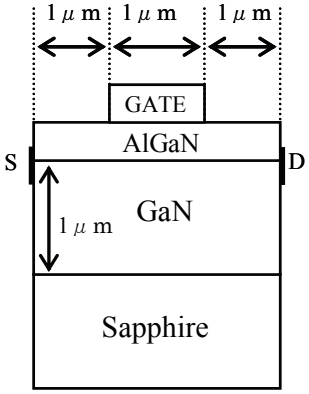

Fig.1. Device structure used for simulation. Trap charges are assumed in 1μm thick GaN buffer layer.

Table.1 Simulated drain currents in transient and steady-states. (mA/mm)

Buffer Type	No trap	ET	HT
Id(Vd=0.1V, t=10ns)	45.6	42.6	35.4
Id(Vd=0.1V, t=∞)	45.6	43.2	38.5
ΔId	0.0	0.6	3.1

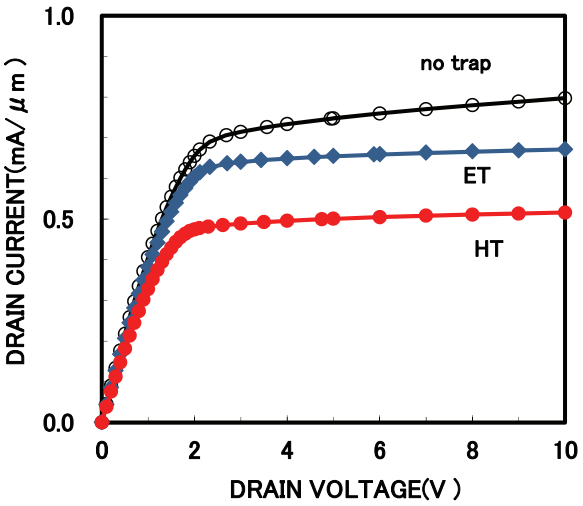

Fig.2. DC Id-Vd characteristics for different buffer layers. Vg = 0 V.

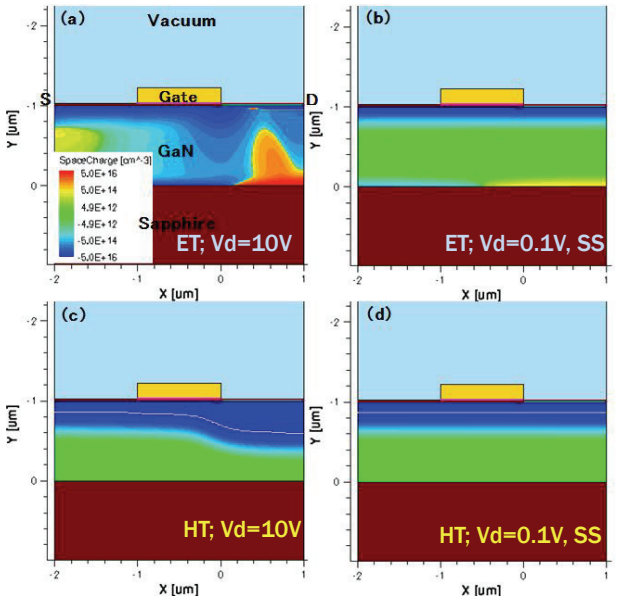

Fig. 3. Space charge distribution profiles. (a) ET; under stress condition (Vd=10V), (b) ET; Vd=0.1V steady-state, (c) HT; under stress condition (Vd=10V), (d) HT; Vd=0.1V steady-state. Blue is negative charge and red is positive charge.

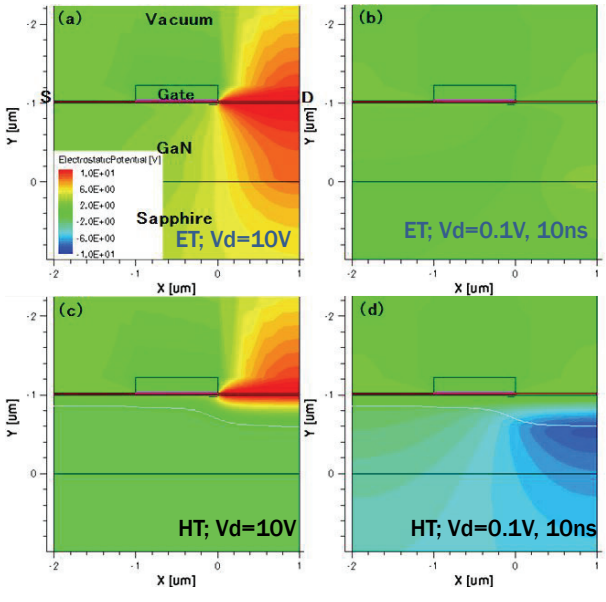

Fig.4. Electrostatic potential profiles. (a) ET; Vd=10V, steady state, (b) ET; Vd=0.1V, 10ns after Vd change, (c) HT; Vd=10V steady-state, (d) HT; Vd=0.1V, 10ns after Vd change. Blue is negative potential and red is positive potential.