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An Al_2O_3/InSb/Si MOS Diode Having an Ultra-Thin InSb Layer

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1. Introduction

Recently, interests for III-V compound semiconductors have been revived for LSIs in the post scaling era. Among them, InSb is one of the most promising candidates because it features highest electron mobility of 78,000 $cm^2/(Vs)$ and highest saturation velocity of $5x10^7$ cm/s. High performance HEMTs based on InSb/InAlSb material system have been already demonstrated [1]. However, growth of high quality InSb on Si is difficult due to the large lattice mismatch of 19.3%. So far, most of the devices reported were grown on GaAs substrates.

We have recently demonstrated that good InSb epitaxial films can be grown on Si (111) substrates using surface reconstruction controlled epitaxy [2]. This technique is based on the fact that the InSb layer grown on a Si (111) substrate is rotated by 30 degrees with respect to the substrate under a certain initial condition, which reduces the lattice mismatch to only 3.3 %, as shown in Fig. 1. Good *C-V* characteristics have also been demonstrated for the MOS diodes fabricated on 1-μm thick InSb epilayers on Si substrates [3]. Moreover, this reduction of the lattice mismatch gives rise to a new possibility, an InSb/Si quantum well (QW) MOSFETs based on an ultra thin InSb layer on Si. If the thickness of the InSb channel layer is equal to or smaller than the critical thickness, such thin channels have good quality. This is possible because the reduction of the lattice mismatch enlarges the critical thickness to a practical value, 5-10 nm, which can be used for the channel of the MOSFET. This has various advantages, such as short growth time, suppression of short channel effect due to strong electron confinement. In this paper, we fabricated and characterized Al_2O_3/InSb/Si MOS diodes with various InSb thicknesses to investigate this possibility.

2. Epitaxial Growth and Diode Fabrication

The details of the growth procedure were reported previously [4, 5]. Here, we describe the essence of the growth technique. A key to rotate the InSb epitaxial layer is the InSb initial bi-layer prepared by adsorption of 1 monolayer (ML) Sb onto In-induced surface reconstruction. Special care is taken here to the phase of the surface reconstruction. The InSb films were then grown by two-step growth procedure on this bi-layer. The growth temperature was 200 C for the first layer, and 440 C for the second layer, respectively.

Epitaxial films having various thicknesses from 10 nm to 1 μm were prepared by this growth technique. The p-type Si substrates having specific resistance of 10-20 Ωcm were used. The grown InSb films were slightly n-type depending on the thickness, though no impurity was intentionally doped.

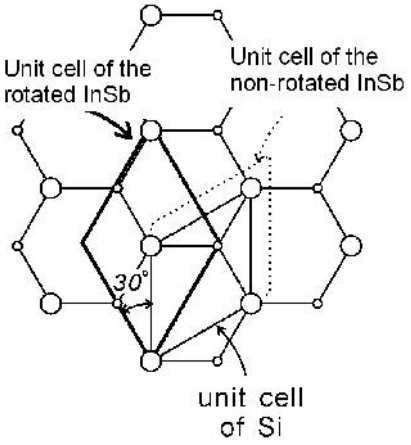

Fig. 1. Schematic view of the Si atoms in a (111) surface with rotated and non-rotated InSb unit cells.

To investigate the possibilities of InSb QW MOSFETs on Si substrates we fabricated Al_2O_3/InSb MOS diodes on epitaxial films grown using above technique. An Al_2O_3 insulator film was deposited by using atomic layer deposition (ALD) at 250 C. Thickness of the Al_2O_3 was 30 nm. Ohmic contacts were fabricated based on Sn/Au/Ni/Ti/Au metals deposited by electron beam evaporation. This is in contrast to our previous work [3], where hole injection from the non-alloyed ohmic contacts were observed.

4. Capacitance-Voltage Characteristics

Figure 2 shows the capacitance-voltage (*C-V*) curves of the fabricated diode having an InSb layer of 10 nm. *C-V* curves were measured at room temperature and 77 K with signal frequencies of 1 MHz. When the applied voltage was 5 V, the capacitances are close to the accumulation capacitance assuming the Al_2O_3 dielectric constant of about 10. The curves are normalized by these values.

The *C-V* curve at RT shows low-frequency behavior with a small dip. On the other hand, n-type high-frequency behavior showing large capacitance drop was observed at 77 K. A most interesting point is that only 10-nm InSb layer directly grown on Si works as a channel layer for a MOS diode. This indicates good quality of InSb layer

grown using surface reconstruction controlled epitaxy technique.

Next, we investigated the effects of InSb thickness on the *C-V* curves. Figure 3 shows the *C-V* curves of the samples with InSb thickness from 50 nm to 1 μm measured at 77 K. The measurements were carried out when decreasing the dc bias voltage. In this thickness range, the magnitude of the variation decreases when decreasing the InSb thickness. It is also shown that the flat band voltage shifts to negative direction when decreasing the layer thickness except for the 50-nm sample. These results are in good accordance with the crystal quality of the epitaxial layers. It is expected that the dislocation density is inversely proportional to the distance from the heterointerface [6]. Because the dislocations in InSb works as donors, the electron density increases when approaching the heterointerface [4]. This should cause the flat band shift.

Figure 4 shows the *C-V* curves of the samples with the InSb thickness from 10 to 50 nm. The curve of the 50-nm sample is plotted again for reference. In contrast to the previous figure, the magnitude of the variation increases when decreasing the InSb thickness. This indicates that the crystal quality improves for thinner InSb layers. This can be explained by the critical thickness. Due to the 30-degree rotation the lattice mismatch reduces to only 3.3 %, which corresponds to the critical thickness of 5-10 nm. When the thickness of InSb is slightly larger than the critical thickness, the dislocation density is expected to decrease when approaching the critical thickness.

5. Conclusions

Al_2O_3/InSb/Si MOS diodes having an ultra thin InSb layer were fabricated on a Si (111) substrate. Owing to the reduction of lattice mismatch, good *C-V* characteristics were demonstrated. This indicates the possibility of the Al_2O_3/InSb/Si QWMOSFET.

Acknowledgements

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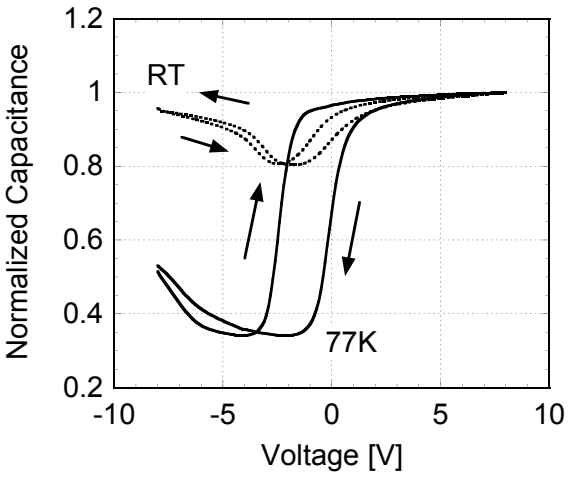

Fig. 2. *C-V* characteristics of the Al_2O_3/InSb/Si MOS diode at R. T. and 77 K. (The thickness of the InSb is 10 nm)

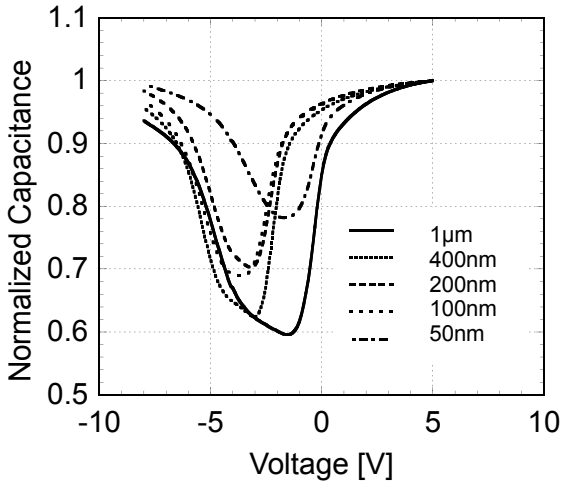

Fig. 3. Dependence of the *C-V* characteristics of the Al_2O_3/InSb/Si MOS diodes on the InSb thickness. (1μm to 50 nm).

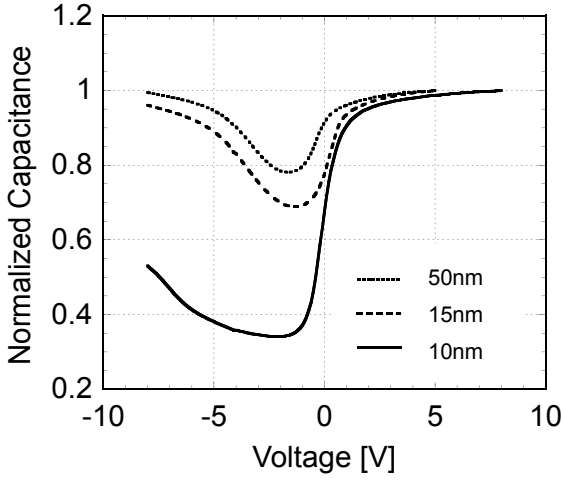

Fig. 4. Dependence of the *C-V* characteristics of the Al_2O_3/InSb/Si MOS diodes on the InSb thickness. (50 nm to 10 nm)