Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp196-197

Effect of Etch Damage on Device performance in Trench-gate and Mesa-gate GaN Vertical MOSFET

Ki-Won Kim[1], Sung-Dal Jung[1], Mi-Kyung Kwon[1], Ryun-Hwi Kim[1], Dong-Seok Kim[1], Ki-Sik Im[1], Hee-Sung Kang[1], Chul-Ho Won[1], Kyu-Il Jang[1], Jae-Hoon Lee[2], Ki-Se Kim[2], and Jung-Hee Lee[1]

[1] Kyungpook National Univ.
1370 Sankyuk 3-dong, Buk-gu, Daegu 702-701, Republic of Korea
Phone: +82-53-950-6555 E-mail: jlee@ee.knu.ac.kr

[2] Samsung LED
314 Maetan 3-dong, Yeongtong-gu, Suwon-City, Gyeonggi-do 443-743, Republic of Korea

1. Introduction

GaN-based semiconductors are the most promising materials for next generation power switching devices due to their remarkable physical parameters such as high breakdown electric field, high saturation velocity, high electron mobility, and good thermal conductivity [1]. Vertical devices are more preferable than lateral ones for discrete high-power switching devices, because vertical ones are more area-efficient. However, etching process during the fabrication gives rise to plasma damage and bad surface morphology. In this work, we investigated effects of surface damage caused by etching which can be modeled as parasitic resistances both in the vertical trench- and the mesa-gate GaN MOSFET. TMAH treatment after etching was proposed for smoothening of surface and found to be efficient in reducing the leakage current.

2. Experimental

The layer structures for the device were grown on sapphire substrate by metal-organic chemical vapor deposition (MOCVD). Layers consisting of Si-doped n^+-GaN layer for drain contact (0.5μm), n^--GaN layer for the drift (1μm), Mg-doped p-GaN for the channel (0.5μm), and Si-doped n^+-GaN for source contact (0.5μm) were grown. The doping densities measured by hall measurement for the n^+-GaN, n^--GaN, and p-GaN are 1×10^{18} , 5×10^{16}, 3×10^{17} cm^{-3}, respectively.

The cross-sectional images of the fabricated trench - and mesa-gate MOSFET are shown in Fig. 1. Etching for the gate and the drain was performed by using Cl_2/BCl_2 gas mixture in inductively coupled plasma (ICP) etcher. Differently from the trench-gate MOSFET, the mesa-gate MOSFET requires etching only for defining gate region. A 38 nm-thick Al_2O_3 layer as gate insulator was then deposited by atomic layer deposition (ALD). Ti/Al/Ni/Au (30/120/40/50nm) contacts are used for the source and drain electrodes, which are formed by the usual lift-off process. As the gate metal, Ni/Au (100/120 nm) is used.

3. Results and Discussion

The I_D-V_D characteristics from the fabricated trench- and mesa-gate MOSFET are shown in Fig. 2. Both devices exhibited threshold voltage of ~ 11 V and the devices were modulated to gate voltage of +15V. The mesa-gate MOSFET demonstrated excellent pinch-off characteristics with drain current of 1.5 mA/mm, but with unstable characteristics at higher gate voltages. On the other hand, the trench-gate MOSFET showed very low drain current of few μA/mm and very bad pinch-off characteristics due to high gate leakage current as shown in Fig 3, approximately 2 orders higher in magnitude compared to the value for the mesa-gate MOSFET.

To determine the mechanisms responsible for the observed drain current and gate leakage current, equivalent electric circuits for the fabricated devices are modeled as in Fig. 4. For the trench-gate MOSFET, we observed severe gate leakage current, caused by roughened surface after plasma etching, which can be represented by large leakage paths, I_{GS} and I_{DG}, through the parasitic resistances between gate and source/drain. This is the reason for the low drain current and bad pinch-off characteristics, because I_{GS} (I_{GD}) is dominated especially at low V_{DS}. On the other hand, the leakage paths are relatively ineffective for the mesa-gate MOSFET, because the etched surface was not totally covered by gate metal and hence the area of the leakage path becomes small compared to that of the trench-gate MOSFET in which the etched area was completely covered with gate metal. It is noticed that electrode configuration in vertical type GaN MOSFETs also can be important in determining the device performance.

We have utilized the TMAH treatment for the purpose of not only smoothing the roughened surface, but also removing the damage caused by plasma etching. The characteristics of both devices after TMAH treatment were shown in Fig. 5. Both devices demonstrated high drain current of 7 mA/mm by good modulation characteristics and low threshold voltage of 5 V by decreased gate leakage current. The gate leakage currents are lower value by reduced surface damage than value of devices before TMAH treatment.

4. Conclusions

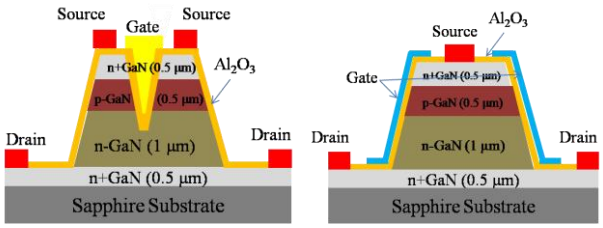
In summary, effect of etch damage on device performance by surface damage in trench-gate and mesa-gate GaN MOSFET have been demonstrated. These devices make large leakage paths through the parasitic resistances due to surface damage, which deteriorate gate leakage current. The device characteristics can be improved by surface smoothening such as TMAH treatment.

Acknowledgements

This work was supported by Samsung LED, 2008 Brain Korea 21 (BK21), the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (No. 2011-0001076), "Survey of high efficiency power devices and inverter system for power grid" project of Korea Ministry of Knowledge Economy, and WCU (World Class University) program through the Korea Science and Engineering Foundation funded by the Ministry of Education, Science and Technology (R33-10055).

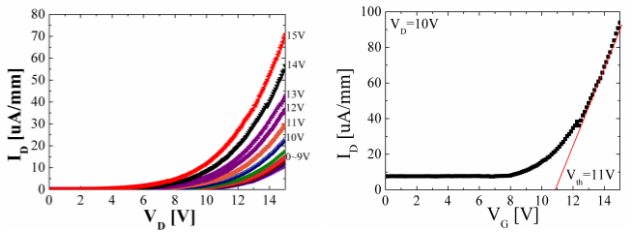
References

[1] T. P. Chow, et al., *Mater. Res. Soc. Symp. Proc.,* Vol. 622, T1.1, 2000.

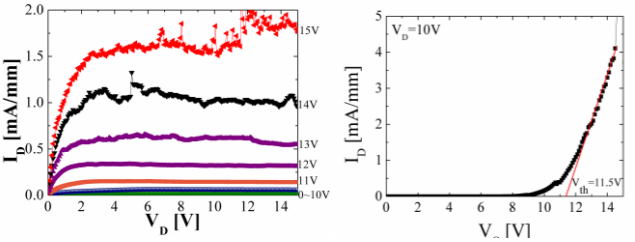


(a) (b)

Fig. 1. Schematic of device structure for (a) trench-gate MOSFET and (b) mesa-gate MOSFET.



(a) (b)



(c) (d)

Fig. 2. ID-VD and ID-VG characteristics of (a),(b) trench-gate MOSFET and (c),(d) mesa-gate MOSFET.

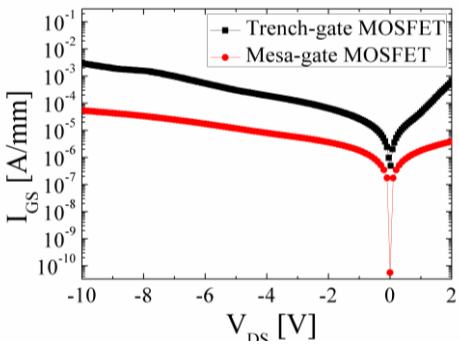


Fig. 3. The gate leakage current of trench-gate and mesa-gate MOSFET.

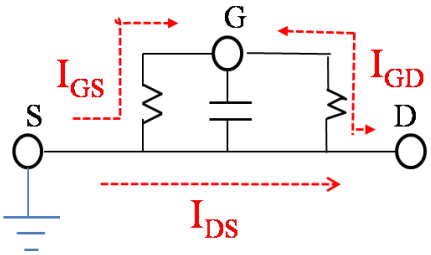
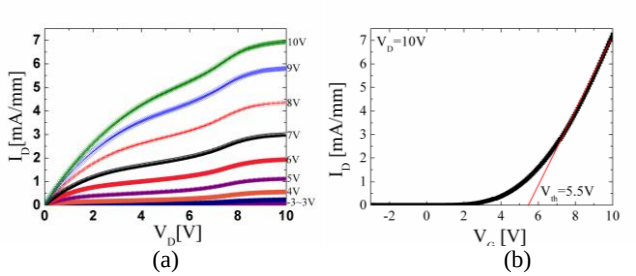
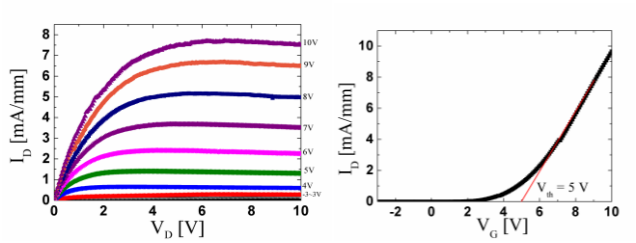


Fig.4. Equivalent electric circuit of modeled devices. (a) trench-gate MOSFET, (b) mesa-gate MOSFET.



(a) (b)



(c) (d)

Fig. 5. ID-VD and ID-VG characteristics of (a),(b) trench-gate MOSFET and (c),(d) mesa-gate MOSFET after TMAH treatment.

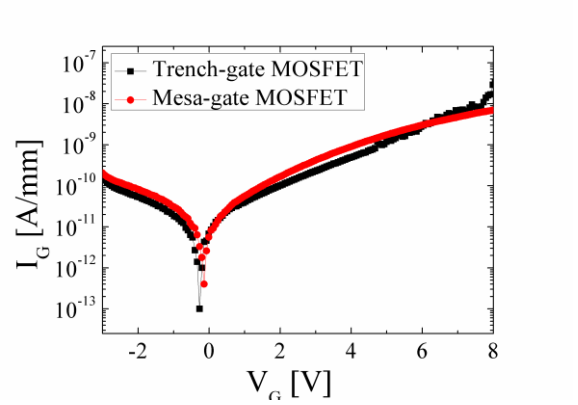


Fig. 6. The gate leakage current of trench-gate and mesa-gate MOSFET after TMAH treatment.