# Performance Improvement of 850nm Si Photodiodes by Symmetric Layout in Standard 0.18 μm CMOS Technology

Fang-Ping Chou, Guan-Yu Chen, Ching-Wen Wang, Zi-Ying Li, Yu-Chang Liu, Wei-Kuo Huang and Yue-Ming Hsin

Department of Electrical Engineering, National Central University,

Jhung-Li, 32001, Taiwan

Phone: +886-3-4227151 ext. 34468 E-mail: yhsin@ee.ncu.edu.tw

# 1. Introduction

Recently there has been a shift in attention from a focus on the electrical interconnections to an emphasis on determining optical communication. Due to low cost-effective, Si material have gathered great importance in recent years. The standard complementary metal–oxide–semiconductor (CMOS) technology compatible photodiode (PD) have been widely used for optical short-distance interconnect. [1]-[4]

However, using standard COMS technology confined the terms of design. Researchers have studied several device layout styles in their search for the best device performance.[5][6]

In this work, different layout geometries of PDs are realized in the standard 0.18 µm CMOS technology without any process modifications. Two new layouts including square and octagon are compared with the conventional rectangle layout. The octagon layout demonstrates higher responsivity of 1.24 A/W for 850 nm wavelength and lower capacitance with improved bandwidth.

# 2. Device Design

The proposed PDs was fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) 0.18- $\mu$ m CMOS technology without process modifications. The multiple p-n diodes in the basic PD design by using the n-well, p-well, shallow trench isolation (STI) oxide as shown in Fig 1. The width of n-well, p-well and STI are 0.86  $\mu$ m , 1.4  $\mu$ m and 0.36  $\mu$ m , respectively. The n-implant (V<sub>R</sub>) is positively biased to reverse bias the p-n diodes and collect the photo-generated carriers. The p-implant is grounded for bias schemes.

Fig. 2 shows the three different layouts of PDs, Fig. 2(a) is a conventional rectangular PD, Fig. 2(b) and (c) are square and octagonal PD which are both symmetric. The size of the active region are  $50 \times 50 \ \mu\text{m}^2$  for the rectangular and square PD and the diagonal of 50- $\mu$ m for the octagonal PD are used to comply with the diameter of the multi-mode fiber.

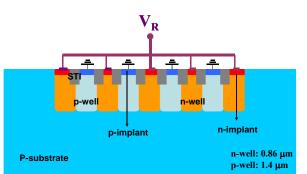


Fig. 1. A schematic cross-section of the basic photodiode showing the  $V_R$  bias to n-implant and grounded to p-implant.

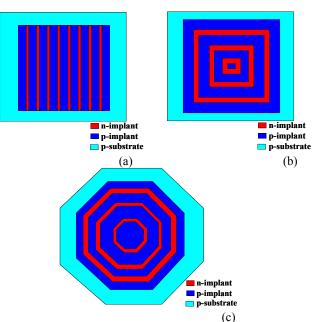


Fig. 2. Device layouts of (a) a rectangular PD and (b) a square PD (c) an octagonal PD  $\,$ 

### 3. Characteristics and discussion

Fig. 3 shows the measured dark currents for proposed PDs. The PDs with symmetric layout have larger break down voltage. The square PD does not have a sharp breakdown behavior, indicating that edge breakdown is occurring. The compared responsivity is shown in Fig. 4. At low bias, the symmetric PDs also have better responsivity than rectangular one. The responsivities for rectangular, square, and octagonal PDs are  $0.06 \text{ A/W}_{\circ}$  0.09

A/W and 0.17 A/W, respectively, at low bias. When PDs are operated in the avalanche region, a higher responsivity of 0.37 A/W (at dark current of 1 $\mu$ A) for both rectangular and square PD and 1.24 A/W for octagonal PD are observed from impact ionization. The curve displays that the octagon is effectively decreasing the edge breakdown of corner and has the best responsivity right before breakdown.

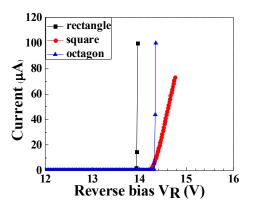


Fig. 3. I–V characteristics of the fabricated PD as a function of  $V_R$  under dark condition in different layouts

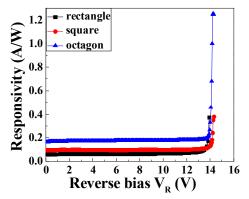


Fig. 4 Measured responsivity of the Si PDs in different layouts.

Fig.5 shows the capacitance-voltage measurement of PDs without illumination by Agilent B1500 with test frequency of 5 MHz. The measured capacitance decreases with the increased  $V_R$  because the depletion region becomes full by degrees. The symmetric octagonal PD demonstrates the smaller capacitance that will be great for improving bandwidth. The -3dB bandwidth measurement is shown in Fig. 6, the octagonal PD shows better bandwidth than the others due to symmetric layout and smaller capacitance. The maximum bandwidth of 2.51 GHz for octagon is obtained.

#### 4. Conclusion

In conclusion, the symmetric layouts of PDs demonstrate higher responsivity and lower capacitance with improved bandwidth. But the square layout is easy to have edge breakdown on the corner leads to degrade performance. The octagonal PD presented the high responsivity of 1.24 A/W and high 3-dB bandwidth of 2.51 GHz due to avalanche multiplication and uniform electric field distribution.

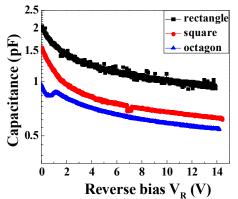


Fig. 5. The measured PD capacitance as function of  $V_R$  in different layouts

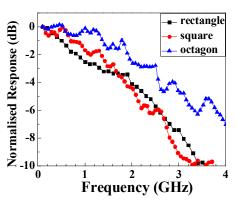


Fig. 6. Measured frequency response of Si PDs in different layouts.

#### 5. References

[1] Sebastian M. Csutak, Jeremy D. Schaub, Wei E. Wu, Rob Shimer, and Joe C. Campbell, "CMOS-Compatible High-Speed Planar Silicon Photodiodes Fabricated on SOI Substrates," IEEE Journal of Quantum Electronics, vol. 38, no. 2, Feb. 2002

[2] Huang, W.K., Liu, Y.C., and Hsin, Y.M, "A high-speed and high-responsivity photodiode in standard CMOS technology," IEEE Photonics Technol. Lett., 2007, 19, pp. 197–199

[3] Koichi Iiyama, Hideki Takamatsu and Takeo Maruyama, "Hole-Injection-Type and Electron-Injection-Type Silicon Avalanche Photodiodes Fabricated by Standard 0.18-μm CMOS Process," IEEE Photonics Technol. Lett., 2010, 22, pp.932–934

[4] Myung-Jae Lee and Woo-Young Choi, "A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain-bandwidth product," Optics Express, Vol. 18, Issue 23, pp. 24189-24194 (2010)

[5] Chia-Sung Chiu, Kun-Ming Chen, Guo-Wei Huang, Ming-I. Chen, Yu-Chi Yang, and Kai-Li Wang, "Capacitance Characteristics Improvement and Power Enhancement for RF LDMOS Transistors Using Annular Layout Structure," IEEE Transactions on microwave theory and techniques, Vol. 59, no. 3, March 2011

[6] P. Lopez, M. Oberst, H. Neubauer, and J. Hauer, "Performance analysis of high-speed MOS transistors with different layout styles," in Proc.Int. Circuits Syst. Conf., May 2005, pp. 3688–3691.