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P-type Tunneling Transistors with Poly-Si by Sequential Lateral Solidification (SLS) Growth Technique

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1. Introduction

Alternative transistor designs which can achieve steeper switching behavior (SS < 60 mV/dec at room temperature) than the MOSFET have been proposed and demonstrated [1-3]. Active-matrix TFT backplane for LCD and OLED applications has been the main trend in the market for flat panel display (FPD), especially Low-Temperature Polycrystalline Silicon (LTPS) thin film transistors (TFTs) have been attracted much attentions. The mobility of poly-Si TFT is much higher than that of amorphous silicon thin film transistor (a-Si TFTs), and indicates higher driving current can be obtained. The applications field of LTPS TFTs will not be only limited to displays but also will also be expanded to IC electronics, driving devices, sensors…etc. In order to realize the applications for LTPS TFTs, the degradation behavior of the devices is an important issue in the applications. However, several degradation mechanisms of LTPS TFTs have already been reported, such as hot carrier effect, self-heating effect, water, contamination, and electrostatic discharge (ESD) [4][5]. In this work, we will develop a planar poly-Si tunneling transistors, and make a comparison with classical TFTs.

2. Devices Fabrication

The LTPS TFTs were fabricated on a corning 1737 glass substrate. At first, a 300-nm-thick TEOS oxide and 50-nm thick hydrogenated amorphous silicon (a-Si:H) layer were deposited at 445 ◦C by a chemical-vapor-deposition (CVD) system. After a dehydrogenation process at 450 ◦C for 2 h, the sample was irradiated at a Lambda Physik LPX 300 excimer laser system just by a two shot of laser with a beam size of 1.6 × 1.6 mm^2 with sequential lateral solidification (SLS) growth technique [6]. The lateral crystallization after completely melting the film in well-defined areas with sharp transitions between liquid and solid silicon produces larger grains than vertical crystallization seeded by solid silicon at the Si-substrate-interface due to near-complete-melt (line beam ELA). The grain size is about 0.5 μm × 3μm, with 50 nm thick poly-Si on glass substrate (Fig. 1). A 100-nm-thick TEOS gate oxide film was deposited by PECVD, and a 300-nm-thick MoW was deposited as gate electrodes. The patterns of the source and drain regions were defined by photolithography. Subsequently, the p-doped & n-doped was implanted by B_2H_6 and PH_3 of ion shower, with the doped conditions are 70keV, 2×10^{15} cm^{-2} and 20keV, 1×10^{15} cm^{-2} for B_2H_6 & PH_3, respectively. The activation temperature for the impurity was by oven at 450℃, 2hr. We estimate the p & n region are about 10^{18}-$10^{20}$$cm^{-3}$. Finally, the metallization process was performed by MoW (300 nm) (Fig. 2 & 3). Furthermore, the classical poly-Si TFT was fabricated together for control devices.

3. Results and discussions

The transfer characteristics (I_{DS}-V_{GS}) of the planar tunneling transistors show ON/OFF ratio ~10^6 (Fig. 4 & 5). The temperature dependence of tunneling current proves that this current is indeed due to the band to band tunneling effect, rather than avalanche effect. The band-to-band-tunneling (BTBT) current in high $|V_G|$ region has much smaller temperature dependence, compared with that in low $|V_G|$ region. The latter is due to thermal Generation-Recombination (thermal G-R) current. The inset of Fig. 4 & 5 shows the top view layout of the planar SLS T-TFT and channel direction with grains. The channel direction is along the longitudinal direction of the poly grain to minimize the scattering by grain boundary (Fig. 4) as compare with that of perpendicular to poly grains (Fig. 5). Therefore, this makes the lower leakage current by thermal G-R in parallel direction devices (Fig. 4). The experimental output characteristics (I_{DS}-V_{DS}) of the tunneling transistors show the higher BTBT current in channel direction parallel to the grain (Fig. 6). Note that the BTBT is not onset with gate voltage -10V and -20V. It is forward bias for p/i/n diode at positive V_{DS}, and the BTBT would be occurred at negative V_{DS} for reverse bias, and the behavior of the p/i/n-diode can be observed at V_G=0 (Fig. 7). While the drain bias switches the device characteristics to reverse-biased of p/i/n diode with a surface Zener tunneling diode. The electrons flow from the p+ doped region into the channel region and tunnel to the n+ doped region for p-type tunneling transistors operation. The stress bias of gate and drain were applied simultaneously, the DC stress conditions are V_{GS} = -25 V and I_{DS} = 1μA. The transfer characteristics data after constant current stress (CCS) shows stable in channel parallel grain devices (Fig. 8 & 9). The threshold voltage shift of tunneling transistors shows more stable than that of classical p-TFTs under DC constant current stress (Fig. 10). The reliability will be improved significantly by the band to band tunneling current, which can effectively reduced the dangling bonds as trap center formation due to reduce carrier velocity and scattering.

4. Conclusions

We have successful demonstrated the novel poly-Si tunneling transistors and examined the reliability. The temperature dependence of tunneling current proves that the current of our device is indeed due to the band to band tunneling effect, rather than avalanche effect. The promising poly-Si tunneling transistors with the gate-controlled current and the low off-current attracts in some applications such as display backplane, 3D-IC memory and microwave circuits in the future.

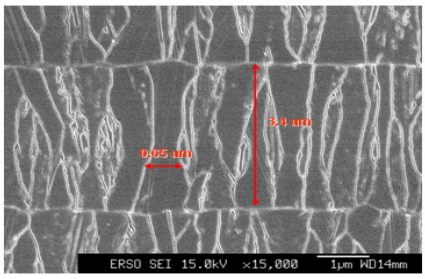

Fig. 1. The SEM image of poly-Si by excimer laser annealing with mask for lateral growth, which called sequential lateral solidification (SLS). The grain size is about 0.5 μm × 3μm, with 50 nm thick poly-Si on glass substrate.

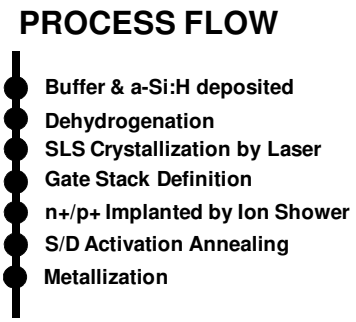

Fig. 2. The process flow of the tunneling transistors with poly-Si by SLS.

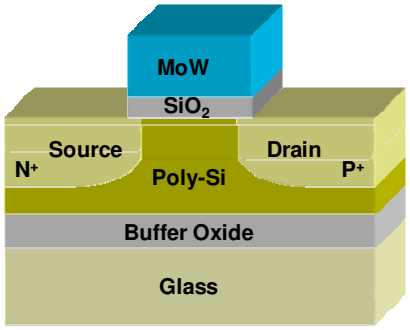

Fig. 3. The structure of poly-Si tunneling transistors with standard gen. II process. The process thermal budget is 450℃.

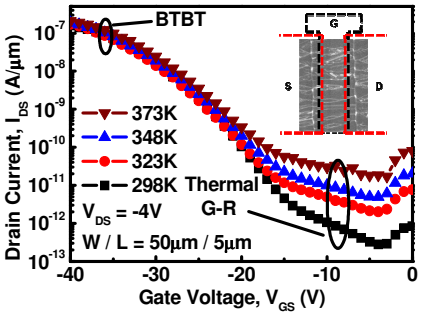

Fig. 4. The transfer characteristics I_{DS}-V_{GS} of p-type tunneling transistors with channel parallel to grains. The ON/OFF ratio is close to 6 magnitudes.

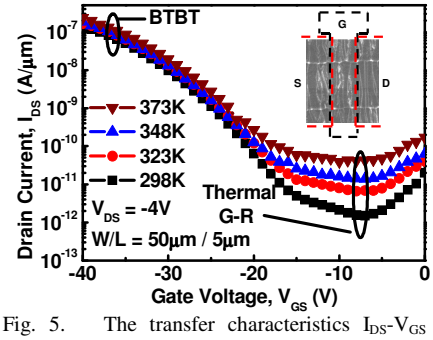

Fig. 5. The transfer characteristics I_{DS}-V_{GS} of p-type tunneling transistors with channel perpendicular to grains. The leakage current is higher than that of channel parallel to grains due to lots of grain boundaries.

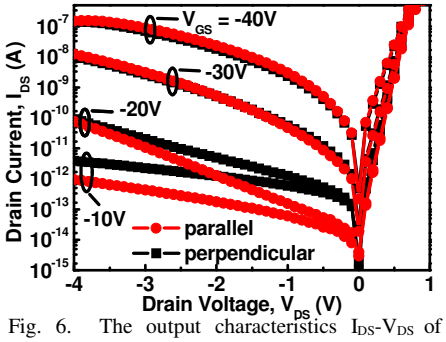

Fig. 6. The output characteristics I_{DS}-V_{DS} of p-type tunneling transistors. It is forward bias for p/i/n diode at positive V_{DS}, and the BTBT would be occurred at negative V_{DS} for reverse bias

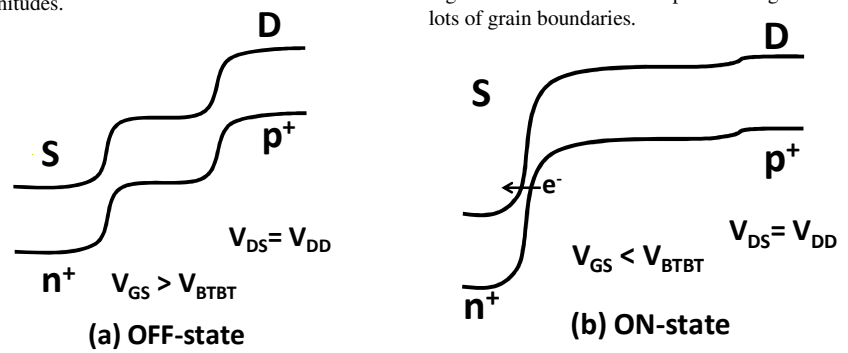

Fig. 7. Band diagram of the p-type tunneling transistors at (a) OFF and (b) ON operation. While the drain bias switches the device characteristics to reverse-biased of p/i/n diode with a surface Zener tunneling diode. The electrons flow from the p+ doped region into the channel region and tunnel to the n+ doped region for p-type tunneling transistors operation.

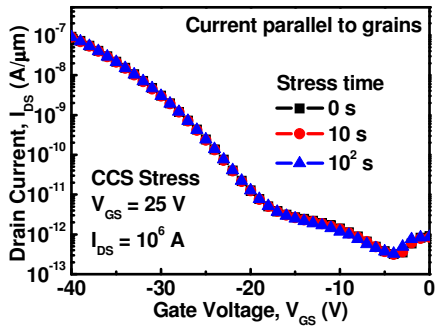

Fig. 8. The transfer characteristics of p-type tunneling transistors with channel parallel to grains under DC CCS.

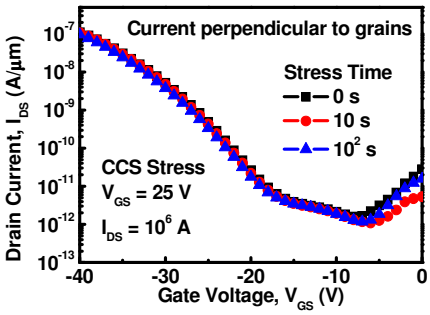

Fig. 9. The transfer characteristics of p-type tunneling transistors with channel perpendicular to grains under DC CCS.

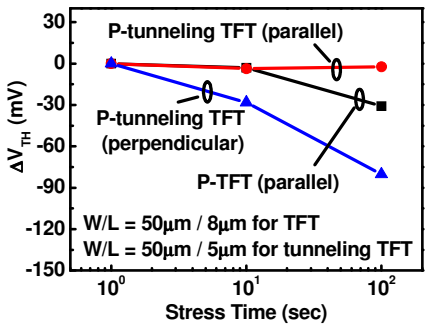

Fig. 10. The threshold voltage stability of tunneling transistors and classical p-TFTs under DC CCS.

5. Acknowledgements

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