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High Speed and High Efficiency Si Optical Modulator with MOS Junction, Using Large-Grain of Poly-Silicon Gate

Junichi Fujikata[1,2], Masashi Takahashi[1,3], Shigeki Takahashi[1,2], Takeshi Akagawa[1,2], Masataka Noguchi[1,2], Tsuyoshi Horikawa[1,3], Takahiro Nakamura[1,2], and Yasuhiko Arakawa[1,4]

[1] Institute for Photonics-Electronics Convergence System Technology (PECST)

[2] Photonics Electronics Technology Research Association (PETRA), West 7 SCR, 16-1, Onogawa, Tsukuba, Ibaraki 305-8569, Japan

[3] National Institute of Advanced Industrial Science and Technology (AIST), West 7 SCR, 16-1, Onogawa, Tsukuba, Ibaraki 305-8569, Japan

[4] Institute of Industrial Science, The University of Tokyo, 4-6-1, Komaba, Meguro, Tokyo 153-8505, Japan

Phone: +81-29-868-6520 E-mail: j-fujikata@petra-jp.org

1. Introduction

Silicon photonics has recently become a subject of intense interest because it offers an opportunity for low cost, low power consumption, and high bandwidth of optoelectronic solutions for applications ranging from telecommunications down to chip-to-chip interconnects [1]. To realize photonics-electronics convergence system, it is highly expected to achieve a high-speed and high-efficiency Si optical modulator (Si-MOD).

As for metal-oxide-semiconductor (MOS) capacitor type of Si-MODs, high efficiency has been achieved by accumulating free-carriers at the gate-oxide/silicon interface [2]. On the other hand, conductivity and propagation loss of poly-silicon (poly-Si) waveguides have been reported to affect the high-speed and optical-loss properties [3].

In this paper, we present a high-speed and high-efficiency Si optical modulator with MOS junction, using large-grain of a poly-Si gate, which contributes to smaller optical loss and higher conductivity.

2. Experiment

Figure 1 shows a schematic diagram of the Si-MOD with a MOS junction. The fabrication process started from 4-inch silicon-on-insulator (SOI) wafers, of which SOI thickness was 220 nm. After 5nm-thickness of gate-oxide was grown by thermal oxidation, an amorphous-silicon layer was deposited by low-pressure chemical vapor deposition and recrystallized by two-step annealing [4]. The Si waveguides (Si-WGs) and poly-Si gates were patterned by electron beam lithography and dry etching. After 1.1μm-thickness of SiO_2 upper-clad layer deposition, contact-holes were formed by i-line lithography and dry-etching process. Finally, stacked electrodes of Ti/TiN/Al layers were deposited and patterned to form RF electrodes. The doping densities of p-Si and n-poly-Si were $1x10^{18}/cm^3$, respectively.

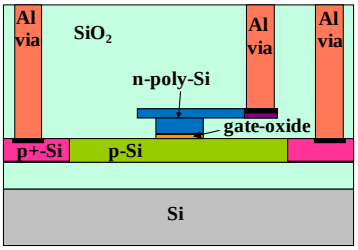

Fig. 1 Schematic diagram of the MOS capacitor type of Si MOD.

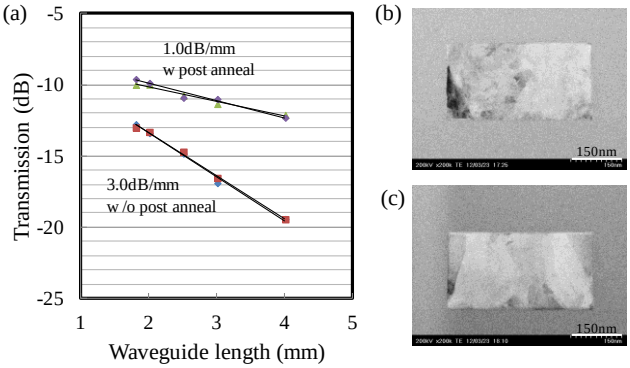

Fig. 2 (a) Optical transmission property and (b) cross-sectional TEM images of poly-Si channel waveguides with and without post-annealing.

3. Results and discussion

First, we studied the optical transmission property of poly-Si-WGs. By two-step recrystallization technique of amorphous silicon, quite a smooth surface with about 1-nm root-mean-square roughness was achieved for the poly-Si-WGs [4]. Figure 2 shows (a) optical transmission property, and (b) cross-sectional TEM images of poly-Si channel waveguides with and without 2nd high temperature post-annealing at 1100℃. The poly-Si WG has the dimension of which height was 220nm and width was 440nm.

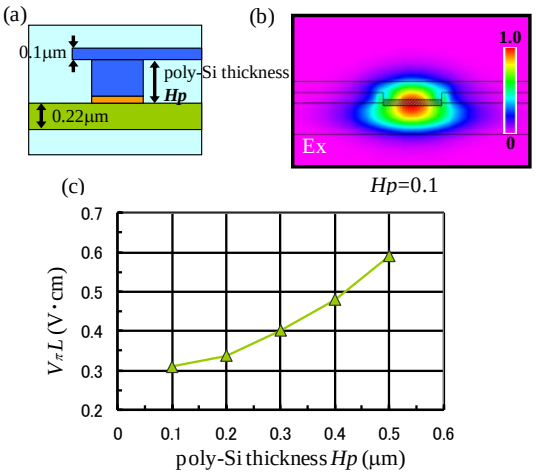

Fig. 3 (a) Schematic diagram of simulation model for the Si-MOD. (b) Contour map of electric field intensity in case of poly-Si thickness (Hp) = 0.1μm. (c) $V_\pi L$ dependence on Hp.

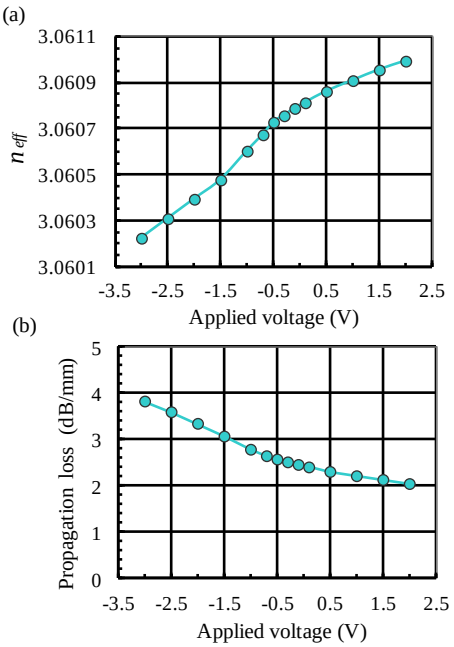

Fig. 4 (a) Effective refractive index (n_{eff}) and (b) optical propagation loss of the Si-MOD with MOS junction dependence on applied voltage to the gate-poly-Si electrode.

The optical propagation loss decreased from 3.0 dB/mm to 1.0 dB/mm by application of post-annealing, which is small enough for the Si-MODs.

From the TEM images, poly-Si layer grains grew into large grains of 200-300 nm diameters, while surface roughness hardly changed after post-annealing. That is, improvement in optical loss should originate mainly from reducing optical absorption at the grain boundary [5]. The post-annealed poly-Si layer with P doping level of 1-5x10^{18}/cm^3 showed also high-conductivity comparable to single crystal with P doping.

The optimum Si-MOD structure of MOS junction was designed by finite-element-method of optical simulation linked with semiconductor device simulation, under the condition that the doping densities for p^+-Si and n-poy-Si are the same for the fabricated device of 1x10^{18}/cm^3 [6]. Figure 3 shows (a) schematic diagram of a simulation model for the Si-MOD, (b) contour map of optical electric field intensity in case of poly-Si thickness (Hp)=0.1 μm, and (c) $V_\pi L$ dependence on Hp. With decrease of Hp, overlap between optical mode field and carrier-density modulation region was improved. In case of Hp=0.1 μm, very high modulation efficiency in $V_\pi L$ of 0.3 V·cm was obtained.

Figure 4 shows (a) effective refractive index (n_{eff}) and (b) optical propagation loss of the Si-MOD with MOS junction dependence on applied voltage to the gate-poly-Si electrode by the simulation. In case of positive applied voltage, free carrier depletion mode was excited. On the other hand, negative voltage induced free carrier accumulation around the gate-oxide/Si interfaces. Around -0.9 V which is comparable to built-in potential at the interface between the gate-oxide and Si, largest refractive index change per applied voltage could be obtained. In this condition, optical absorption loss of free carrier plasma

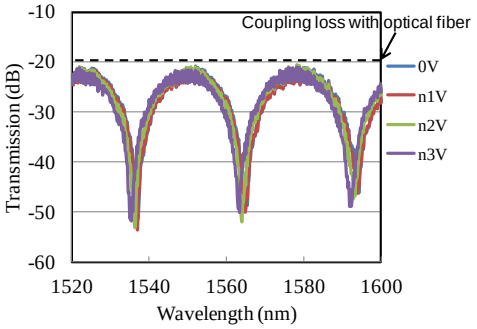

Fig. 5 Transmission spectra of asymmetric MZI structure of the Si-MOD with MOS junction dependence on dc applied voltage.

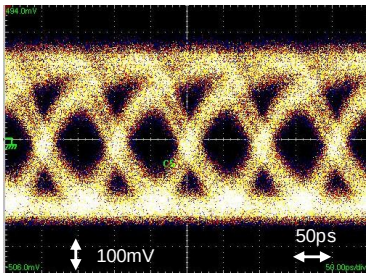

Fig. 6 Measured eye diagram at 10 Gbps with 2^7-1 PRBS.

dispersion effect was about 2.6 dB/mm.

Finally, we measured the fabricated Si-MOD with MOS junction. The Si-MOD had an optimum Hp of 0.1 μm, and the phase shifter length was 200 μm. Figure 5 shows transmission spectra of an asymmetric MZI structure of the Si-MOD with MOS junction dependence on dc applied voltage. With increase of negative dc applied voltage from -1 V to -3 V, about 2.0 nm of spectrum-shift was observed and free spectrum range was 27.8 nm. Modulation efficiency $V_\pi L$ of 0.306 V·cm was obtained, which is very much coincident with the simulation results and is the highest modulation efficiency than those previously reported in the Si-MODs with MOS junction.

Figure 6 shows a measured eye diagram at 10 Gbps with 2^7-1 PRBS under the condition that dc applied voltage was -1.5 V and RF drive voltage was 2.5 V_{pp}. Insertion loss was -3.2 to -4.2 dB and extinction ratio was about 5dB.

4. Conclusions

We developed a high speed and high efficiency Si-MOD with MOS junction, by applying the low optical loss of poly-Si gate with large grains. We designed the optimum Si-MOD structure, and demonstrated very high modulation efficiency of 0.3 V·cm, which is the most efficient in the Si-MODs with MOS junction, and also high speed of 10 Gbps operation.

Acknowledgements

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