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The impacts of ArF Excimer Immersion Lithography on Integrated Silicon Photonics Technology

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1. Introduction

Silicon photonic technology using silicon wire waveguide with high index contrast has been expected to realize integrated photonic devices with compact footprint. In such photonic devices, line edge roughness (LER) and the width deviation (ΔW) in silicon core patterns should be kept at lower levels, in order to satisfy the requirements for decreasing propagation loss and refractive index fluctuation. The usage of high-resolution lithography in device fabrication is apparently a key issue for these requirements. ITRS roadmap showing lithography trends for resolution and gate width control in CMOS technology is shown in Fig.1. ArF immersion lithography is clearly the best technology currently available in terms of ΔW control.

In this paper, we report the silicon photonic device fabrication by using high-resolution ArF immersion lithography. Then, we also experimentally demonstrate its applicability to wavelength division multiplexing (WDM) devices.

2. Requirements for LER and ΔW in photonic devices

The LER arises from the nature of chemically amplified photoresist and the plasma damage through dry etching [1]. The major propagation loss in waveguide is resulted from the scattering caused by LER. The waveguide scattering loss has been reported to proportionally increase with the square of LER [2]. The LER should be reduced to around 4 nm for the scattering loss less than 1 dB/cm, in the case of the waveguide whose width is 440 nm and the height is 220 nm.

The fabrication tolerance of waveguide width is also an important issue, because, as is well known, the equivalent index and group index vary as functions of waveguide width [3]. The spectrum shift of silicon photonics devices due to these index variation has a strong impact on the WDM system. For example, the pass band width for a typical wavelength filter is specified as ± 6.5 nm, for coarse WDM (CWDM) systems with 20 nm spacing. The resonance peak shift of a single ring resonator (RR) is calculated for the case of $d\lambda/dw$ of 1.45 and shown in Fig.2. The effect of side wall roughness is ignored for the calculation. To keep the resonace peak shift within ± 6.5 nm, ΔW of the RR must be less than 4.5 nm.

3. LER and ΔW control by ArF Immersion Lithography

Figure 3 shows the contour plot of LER and width variation of 440-nm-wide waveguide photoresist patterns on a 300 mm silicon on insulator (SOI) wafer. Multi-layer resist processes with SiN/SOC/SOG structure are conducted in ArF immersion lithography. In the most of wafer areas, LER meets the 4-nm requirement as discussed in the previous section. The average value of ΔW in Fig.3 (b) is 2.5 nm, which is significantly smaller than the CWDM specification of 4.5nm.

We should consider the influence of the optical proximity effect (OPE) for silicon photonics devices since some distinctive patterns are not found in conventional CMOS devices. Figure 4 shows a photonic crystal line defect waveguide [4,5] without OPE with the hole diameter of 230 nm. The hole diameter deviation of 2 nm is significantly smaller than the previously reported value of 5nm with ArF dry lithography process [6]. The relatively large numerical aperture of 1.3 in ArF immersion lithography apparently reduces OPE and contribute to high-fidelity patterning with the gap width of around 200 nm.

4. Characterization of photonic devices

Silicon wire waveguides and photonic devices were fabricated on 300 mm SOI wafer with 2-μm-thick buried oxide (BOX) layer. Using photo-resist patterns, SOI layer was removed by ICP dry etcher with an HBr-Cl_2-O_2 gas mixture. A 2-μm-thick SiO_2 overclad layer was deposited on the silicon wire waveguide by PECVD. The waveguide width and height are 480 nm and 210 nm, respectively.

Figure 5 shows the transmission spectra of three directional couplers (DCs) with 200 nm gap. The dip wavelength is 1528 nm, and the extinction ratio (difference between bar and cross transmittance) is -25 dB. The dip wavelength is in good agreement with the theoretical value obtained by mode coupling theory and its variation from chip to chip within a wafer is small. This large extinction ratio indicates that the average width and the gap along the waveguide of DC are uniform and further imply that ArF

immersion lithography is capable of realizing demanding interferometric devices such as RR, Mach Zehnder interferometer and an arrayed waveguide grating.

Figure 6 shows the normalized transmittance spectra of four race track type RRs with 10 μm radius. The free spectral range of the RR is around 4.5 nm at 1.5-μm wavelength band. The resonance peak shift is 1.2 nm, which corresponds to ΔW of 0.8 nm according to Fig.2. This result clearly shows that the chip-to-chip width variation is sufficiently small for CWDM systems.

5. Conclusions

ArF immersion lithography is a promising candidate for silicon wire photonic device fabrication due to its precise control of LER and ΔW. The LER of 4 nm and the ΔW of 3 nm were experimentally confirmed over 300mm SOI wafers. Silicon photonic WDM devices such as a DC and a RR were successfully demonstrated.

Acknowledgements

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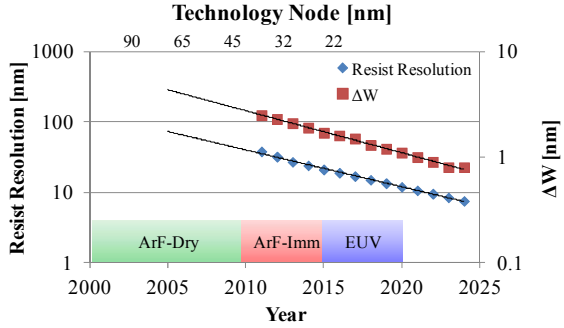

Fig.1. Progress of resist resolution and width deviation. cf. ITRS roadmap 2011.

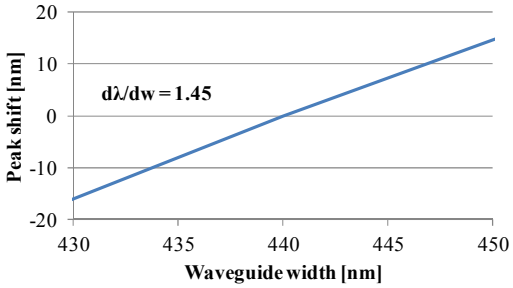

Fig.2. Calculated resonance peak shift as function of waveguide width for RR without side wall roughness.

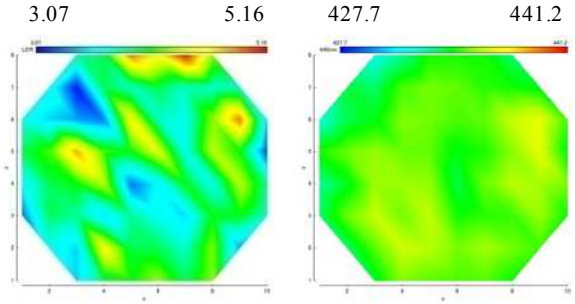

Fig.3. Contour plots for (a) LER and (b) width of 440-nm-wide waveguide patterns fabricated by ArF immersion lithography on 300 mm SOI wafer.

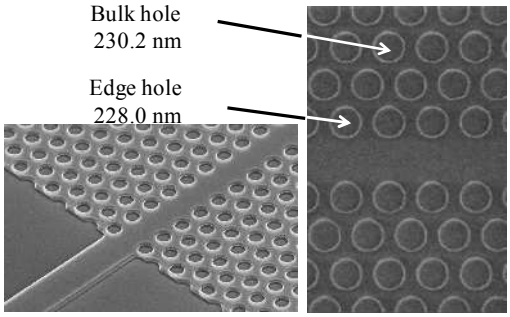

Fig.4. Photonic crystal line defect waveguide fabricated by ArF immersion lithography without optical proximity correction; (left) birds-eye view and (right) top view.

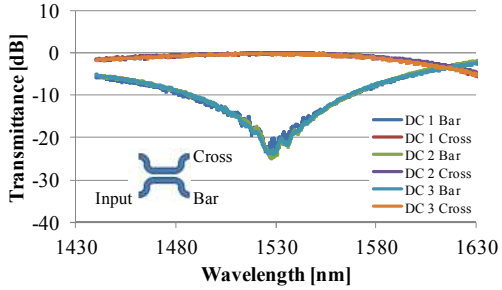

Fig.5. Three DCs transmission spectra of TE polarization in the range from 1440 to 1630 nm. The gap width is 200 nm and the coupling length is 23 μm.

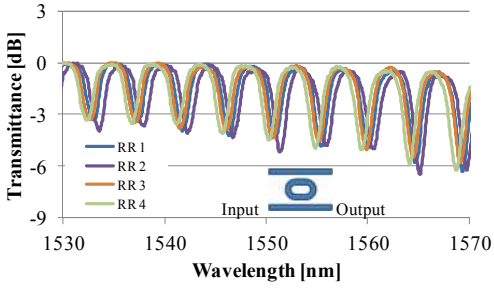

Fig.6. Four RRs normalized transmittance spectra of TE polarization at 1.5-μm wavelength band. The ring radius is 10 μm and the coupling length is 30 μm