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Generic Integration Processes for InP based Application Specific Photonic Integrated Circuits (ASPICs) in Europe: Current Status and future Prospects.

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1. Introduction

In 2004 the FP6 Network of Excellence ePIXnet started with a large number of academic and industrial members on an ambitious mission: to move from a model of independent research to a model of integrated research with shared use of expensive technological infrastructure. After experimenting for two years with facility access activities the ePIXnet Steering Committee published a vision document about a foundry model in Micro- and Nano photonics. Two major integration technologies were identified: InP-based and Silicon Photonics technology. For both technologies a platform organization was established; JePPIX for InP-based integration technology and ePIXfab for Silicon Photonics.

The JePPIX platform has started with providing small scale access for research purposes to the Generic InP-based Photonic Integration technology developed by the COBRA Research Institute of the Eindhoven University of Technology, which is the coordinator of JePPIX. Presently a number of JePPIX partners are working in two large EU-programs (EuroPIC and PARADIGM) on transferring the generic approach from an academic research environment to an industrial foundry environment, in particular the fabs of Oclaro and the FhG Heinrich Hertz Institute. If successful, these projects may bring Europe the first semi-commercial photonic InP-foundry access in or shortly after 2014[1].

Figure1 shows the Generic Technology landscape in Europe with a total R&D effort in InP-Based technology of more than 25M€ and more than double for all three technologies.

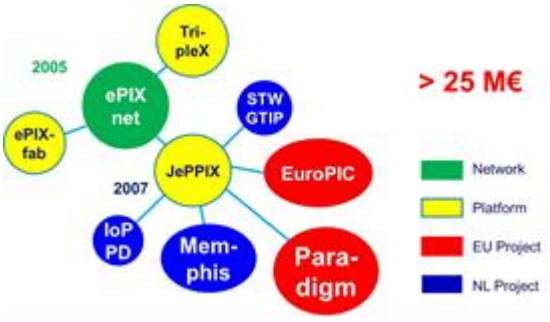

Figure 1: The Generic Technology landscape in Europe.

In this paper we describe the COBRA generic integration Process, which is representative for the industrial foundry processes that will become available later, the current status and our view on the future prospect of a generic InP foundry model.

2. The COBRA generic process

The COBRA Generic Technology presently supports integration of four Basic Building Blocks: Passive Waveguide Devices (PWD), Phase Modulators (PHMs), Semiconductor Optical Amplifiers (SOAs) and Isolation Sections. Polarization converters and Spot size Converters are under development.

The total process consists of more than 200 process steps, which can be grouped into 4 process modules.

1. First module is the Active/Passive integration which results in a fully planar wafer in 3 epitaxial steps and a definition of the active and passive regions with a litho/etching process. An overview of the layer stack in the active as well as the passive regions is given in figure 2.

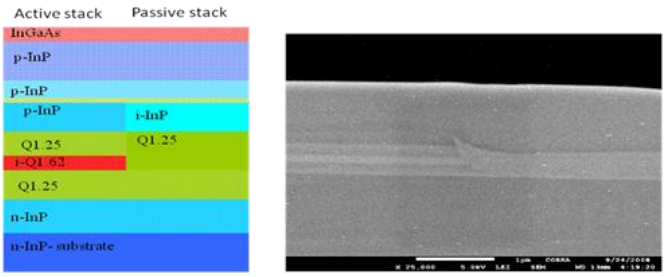

Figure 2: Layer stack in Active/Passive region (left) and SEM picture of a real butt joint coupling

2. Next module is the definition and etching of all waveguides. Depending on which Basic Building Blocks are in the design of the ASPIC this group contains 4 or 5 etching steps. The full waveguide layout of the ASPIC is formed as well as the heights of the waveguides are defined in this process module (figure 3).
3. After the definition of the waveguides the metallization for the SOA's and PHM's need to be added. This starts with a planarization of the wafer either with BCB or Polyimide and via lift off technique the metallization pattern is defined. This part ends with the plating on the p-side and metallization of the n-side of the wafer.
4. The total processing ends with the separation, coating and testing of the different test structures and ASPICs on the wafer.

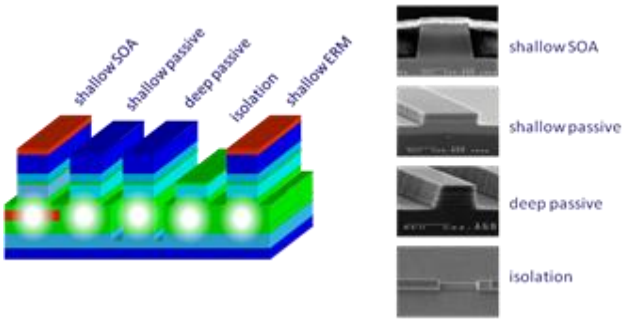

Figure 3: Overview of building blocks with SEM pictures.

With this Generic Integration Technology designs of multiple users can be combined using so-called Multi Project Wafer runs (MPW runs). An example of such a MPW is given in figure 4 in which the 3 most left sections in each quarter represent test structures and the next two columns are reserved for designs from different users, which have cells of about 4x4 mm^2 for their designs. These designs can be made independent from each other.
COBRA is offering small scale access to these MPW's to gain experience with the Generic Foundry approach. In the presentation some applications in different fields will be shown.

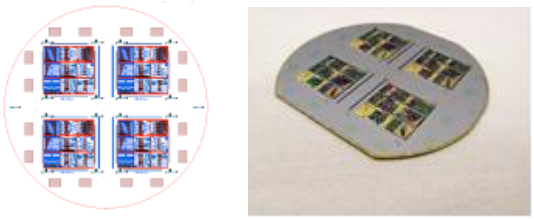

Figure 4: Example of MPW run: Mask set (left) and real processed wafer (right)

3. Current Status and future prospects

As stated above, COBRA is offering small scale access to the MPW runs in the COBRA platform. In the meantime OCLARO and FhG Heinrich Herz Institut are running MPW runs within the European Projects EuroPIC and PARADIGM. In figure 5 examples are given from MPW mask layouts integrating a number of different designs.

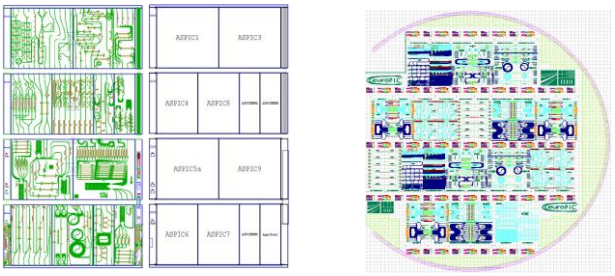

Figure 5: MPW run examples from OCLARO (left) and FhG HHI (right)

As given in figure 6 we expect that the InP_based MPW-runs will become available to external users on a pre-commercial basis already in 2013. The figure shows the roadmap made by the JePPIX consortium, starting with the first generation (G1) COBRA process, followed by projects based on industrial fabs (G1 and G2)[2]. On the long term we foresee integration of a photonics and electronics in a thin InP-based membrane on top of a CMOS wafer (G3, IMOS: InP Membrane on Silicon).

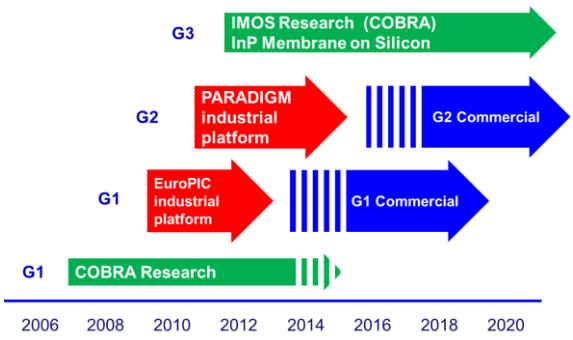

Figure 6: JePPIX Generic Foundry Process Roadmap.

In figure 1 we sketched the Generic Integration Landscape in Europe. At the moment projects are running with a total budget for more than 25M€, with subsidy from the EU and Dutch government. In the near future new programs will be launched in Europe as well as in the Netherlands and there will be place for further development of the current platforms as well as for next generation platforms like IMOS.

4. Conclusion

In Europe we are building an infrastructure for Generic Photonics Integration processes similar to what we saw in the past in the electronics industry with the CMOS process. This will lead to a lot of new applications because the entry costs for small companies will be much lower with respect to a complete development of new chips based on application-specific processes. In Figure 7 we give an indicative example of the entry costs as well as the chip costs per mm^2 in different fab models.

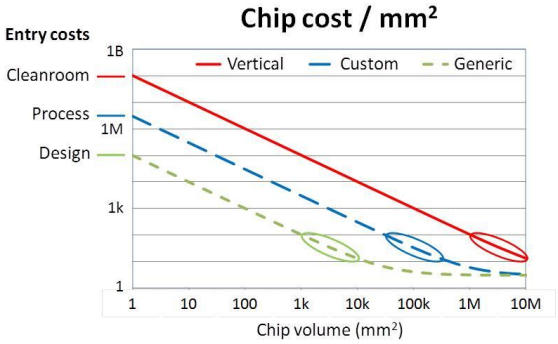

Figure 7: Entry and Chip cost in different fab models

[1] M.K. Smit et al., "Generic foundry model for InP-based photonics", IET Optoelectron., Vol. 5(5), pp. 187–194 (2011)
[2]JePPIX Roadmap 2012, http://www.jeppix.eu/document_store/JePPIX_Roadmap_2012.pdf