Undercut GaAs/In$_{0.5}$Ga$_{0.5}$P High-Speed Laser Power Converter for Simultaneous 10 Gbit/sec Data Detection and Efficient dc Electrical Power Generation

Jhih-Min Wun, Jin-Wei Shi[*], Cheng-Yo Tsai, and Yue-Ming Hsin

Department of Electrical Engineering, National Central University, Taoyuan, 320, Taiwan.
*Phone: +886-3-4227151-34466 ; *E-mail: jwshi@ee.ncu.edu.tw

1. Introduction

Global network data traffic continues to grow, driven primarily by mobile data and internet video. By taking a look at the network equipment energy consumption breakdown, data center network equipment is expected to become the major power consumer [1]. The development of optical interconnect (OI) techniques [2,3] provides an attractive way to further reduce the carbon footprint of data centers. However, the dc component of the high-speed optical data signal at the receiving end of OI system is usually wasted due to the fact that in traditional p-i-n photodiodes (PDs), reverse bias operation is necessary for high-speed performance, which will result in extra power consumption with excess heat generation. In this paper we demonstrated a high-performance GaAs/In$_{0.5}$Ga$_{0.5}$P LPC [4,5], which can generate (instead of consuming) dc electrical power during high-speed data detection in an OI system [4,5]. By using the under-cut mesa to reduce the junction capacitance of device under forward bias operation, we can achieve 10 Gbit/sec error-free operations under +0.4 V forward bias voltage, which corresponds to ~ 10% optical-to-electrical dc power generation efficiency.

2. Device Structure and Fabrications

The inset in Figure 1 (a) and Figure 1 (b) shows a top-view and conceptual cross-sectional view of the fabricated device, respectively. We adopted the structure of a typical vertical-illuminated photodiode with an active circular mesa and a p-type aluminum ring contact on the top. The diameter of the whole mesa and the inner circle for light illumination were 34 μm and 15 μm, respectively. The epi-layer structure, from top to bottom is composed of a 50 nm In$_x$Ga$_{1-x}$As p$^+$ (1×10^{19} cm^{-3}cm^{-3}) ohmic contact layer, a 50 nm Al$_{0.3}$Ga$_{0.7}$As p$^+$ (3×10^{18} cm^{-3}) diffusion blocking layer, a 650 nm GaAs p-type P layer with a graded doping profile (1×10^{19} cm^{-3} (top) to 5×10^{16} cm^{-3} (bottom)), a 730 nm In$_{0.5}$Ga$_{0.5}$P n-type C layer with a graded doping profile (1×10^{16} cm^{-3} (top) to 5×10^{18} cm^{-3} (bottom)), a 100 nm n$^+$ GaAs (6×10^{18} cm^{-3}) and a 300 nm n$^+$ Al$_{0.2}$Ga$_{0.8}$As (1×10^{18} cm^{-3}) bottom ohmic contact layer. The graded doping profile induced built-in electric (E) field in P and C layers can accelerate the electron diffusion/drift process, which would significantly benefit the high-speed performance of our LPC operated under forward bias with a very-small net E-field inside [4,5]. Although the use of graded n-type doping in our collector layer would increase the junction capacitance and degrade the RC-limited band
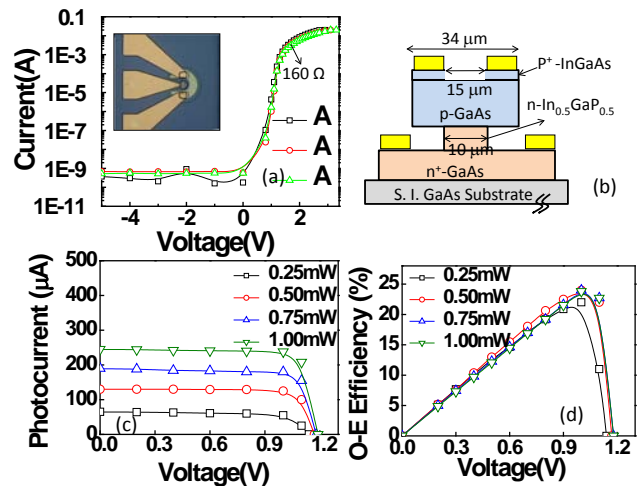

Figure 1. The (a) dark I-V curves, (b) conceptual cross-sectional view of device with undercut mesa, (c) photocurrents measured under different optical pumping powers and forward voltages for devices A (open symbols), and (d) corresponding dc O-E power conversion efficiency. The inset to (a) shows the top-view of the demonstrated LPC.

width, compared with those of device with an undoped collector layer [4], such problem can be minimized by using the In$_{0.5}$Ga$_{0.5}$P mesa with undercut structure, as will be discussed latter. Furthermore, as compared to our previous work using the Al$_{0.2}$Ga$_{0.8}$As layer as collector layer [4], the In$_{0.5}$Ga$_{0.5}$P collector layer can greatly minimize the conduction band offsets between the P and C layers, which would block the electron current and seriously limits the speed performance of LPC [4]. In order to further reduce junction capacitance without seriously reducing the device active area and increasing the differential resistance, an undercut mesa profile (as shown in Figure 1 (b)), has been realized in our device [5]. By properly controlling the wet-etching time, the active diameter of the final fabricated device is around 10 μm, as specified in Figure 1 (b). The detail fabrication processes of our device can be referred to in our previous work [4,5]. The fabricated device is integrated with a co-planar waveguide (CPW) pad on the semi-insulation GaAs substrate for on-wafer measurement.

3. Measurement Results

Figure 1 (a) shows the measured current (I)-voltage (V) curves of device with undercut mesa profile. As can be seen, the differential resistance is around ~160 Ω, which is close to the reference device without under-cut profile [5].

We can expect an improved RC-limited bandwidth for un-dercut device due to the fact that the total resistance (R) should include the external 50 Ω load during measurement and the reduction in C_j should have more obvious influence on enhancing the net RC-limited bandwidth of device [5]. The measured dc photocurrent of our LPC versus the for-ward voltage under different optical pumping power with wavelength at 830 nm are shown in Figure 1 (c) and the corresponding O-E power conversion efficiency is shown in Figure 1 (d). As can be seen, the maximum O-E con-version efficiency happens at the bias as around +1.0 V and the corresponding maximum conversion efficiency is ~23% , which is higher than that of the same under-cut de-vice reported in our previous work [5]. Higher conversion efficiency of our demonstrated LPC can be expected by inserting a distributed Bragg reflector with central wave-length at around ~830 nm below the active layers of device [4] to enhance its photo-absorption process.

The dynamic performance of the device is characterized utilizing a lightwave-component-analyzer (LCA) system with a semiconductor laser at 830nm as the light source. Figure 2 (a) and (b) shows the measured O-E response (f_{O-E}) of device with under-cut (device A) and reference device without undercut (device B), respectively, under a fixed output photocurrent (~90 μA) and two different operating voltages (-5V and +0.8 V). Under +0.8 V operation, the corresponding maximum conversion efficiency is up to ~ 20%. As can be seen for device A, even when the oper-ating voltage is pushed to near turn-on point, the degrada-tion in speed is not so serious (10 to 8 GHz). On the other hand, device B exhibits a more serious degradation in speed performance (9 to 2 GHz) due to its larger junction capaci-tance than those of device A.
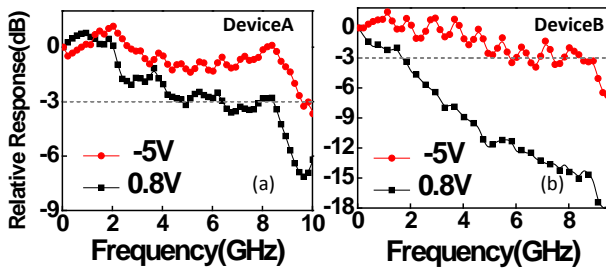

Figure 2. Measured O-E frequency responses of (a) device A and (b) device B under +0.8 V and -5 V under a fixed photocurrent (90 μA).

Figure 3 shows all the measured 3-dB O-E bandwidths under different forward voltages and output photocur-rents. Based on these dynamic measurement results, we can conclude that the demonstrated undercut mesa structure of the $In_{0.5}Ga_{0.5}P$ collector layer can greatly improve speed performance under a forward operating voltage, which usually accompanies a thin depletion layer with a large C_j and serious RC-limited bandwidth.

Figure 4 (a) to (c) shows the measured 10 Gbit/sec eye-patterns of device A under 0, +0.4, and +0.8 V oper-ation, respectively.
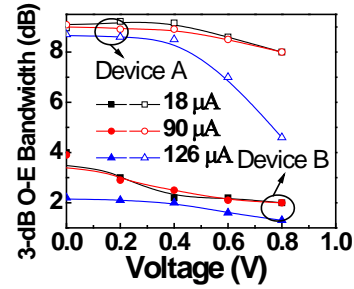

Figure 3. The measured 3-dB O-E bandwidths of these two de-vices under different operating voltages and photocurrents.

We can clearly see that the quality of measured eye-pattern degrades slightly when the forward bias in-creases from zero to +0.8 V and the error-free operation can be achieved when the operation voltage is below +0.4 V.
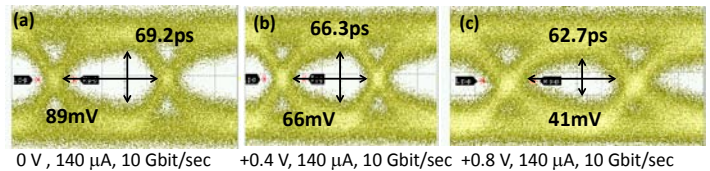

Figure 4. Measured 10 Gbit/sec eye-pattern of device A under different forward biases (a) 0 V; (b) 0.4 V; (c) 0.8 V.

3. Conclusions

We demonstrated a novel LPC. By utilizing the un-dercut mesa with a very small conduction band offset be-tween P (GaAs) and C ($In_{0.5}Ga_{0.5}P$) layers, the demonstrat-ed device can greatly release the RC-limited bandwidth and sustain the high-speed (~9 GHz) performance from zero to near turn-on (0.8V) operating voltages with a ~20 % O-E conversion efficiency. 10 Gbit/sec error-free operation with a ~ 10 % conversion efficiency is achieved. This result changes the common belief that high-speed PDs must be a power-consuming device under reverse bias.

References

[1] C. Lange, D. Kosiankowski, R. Weidmann, and A. Gladishch, "Energy Consumption of Telecommunication Networks and Related Improvement Options," *IEEE J. of Sel. Topics in Quantum Electronics,* vol. 17, pp.285-295, March/April, 2011.

[2] K. Kurata, "High-Speed Optical Transceiver and Systems for Optical Interconnects," *Proc. OFC 2010, San Diego*, CA, USA, March, 2010, pp. OThS3.

[3] J. A. Kash, A. F. Benner, F. E. Doany, D. M. Kuchta, B. G. Lee, P. K. Pepeljugoski, L. Schares, C. L. Schow, M. Taubenblat, "Optical Interconnects in Exascale Supercomputers," *IEEE Photonic Society Meeting 2010,* Denver, Colorado, USA, Nov., 2010, pp. WR1.

[4] J.-W. Shi, F.-M. Kuo, Chan-Shan Yang, S.-S. Lo, and Ci-Ling Pan, "Dynamic Analysis of Cascade Laser Power Converters for Simultaneous High-Speed Data Detection and Opti-cal-to-Electrical dc Power Generation," *IEEE Trans. Elec-tron Device.* vol. 58, pp. 2049-2056, July, 2011.

[5] Jin-Wei Shi, Cheng-Yo Tsai, Chan-Shan Yang, Feng-Ming Kuo, Yue-Ming Hsin, J. E. Bowers, and Ci-Ling Pan, "GaAs/$In_{0.5}Ga_{0.5}P$ Laser Power Converter with Undercut Mesa for Simultaneous High-Speed Data Detection and dc Electrical Power Generation," *IEEE Electron Device Lett.,* vol. 33, pp. 561-563, April, 2012.