

P-I-N Ge on Si Photodiodes for high speed and low power consumption receivers

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1. Introduction

The photodetector is one of the building blocks needed for the implementation of fast silicon photonics integrated circuits. The main considerations for the design of such a device are the bandwidth, the power consumption and the responsivity. Germanium is now considered as the ideal candidate for fully integrated receivers based on SOI substrates and CMOS-like processes [1]. High speed and high responsivity Ge photodiodes have already been reported in literature [2-4]. They however suffer from relatively high dark currents as compared to their III-V homologues. Bias voltage increase directly leads to higher bandwidth but also to a higher dark current mainly through tunneling, as a consequence of Ge low bandgap. Moreover Ge on Si suffers from crystal defects due to the lattice mismatch between Si and Ge.

This paper reports on low power and high speed Germanium photodiodes integrated in Si waveguides for telecom and datacom applications. We present very low dark current (25nA @-1V) and high bandwidth Ge on Si lateral p-i-n photodiodes. Those photodiodes exhibit responsivity of 0.5A/W at 1.55 μ m, and a bandwidth over 40GHz at zero bias.

2. Device Fabrication

Design considerations

Several coupling schemes and diodes structures can be considered for waveguide integration of Ge photodiodes. As butt coupling offers more efficient absorption, the device length can be reduced as seen from the Beam Propagation Method (BPM) simulations in Fig. 1, and consequently the capacitance will be lower, and will not affect the bandwidth. To limit the process complexity for a fully integrated photonic circuit, lateral p-i-n junction is more suitable: contacts are on the same level and topology is limited. To allow fast speed photodiode operation at low reverse bias or zero bias, the internal built-in electric field must be as high as possible. Hence, intrinsic region has to be the narrowest. However, the absorption efficiency which is directly linked to the optical coupling from Si waveguide to Ge layer is degraded. Thus, the intrinsic region width is chosen to be 0.5 μ m to match with the waveguide width, leading to high internal electric field. Final design cross-section of the lateral p-i-n photodiode is represented with dimensions in the Fig. 2.

Fabrication

Starting from 200mm SOI wafers with 2 μ m Buried Oxide (BOX) and 220nm top Si, waveguides and fiber couplers are defined using 193nm Deep-UV lithography followed by HBr dry etching down to the BOX, resulting in 500nm wide and 220nm height Si waveguides. An 800nm thick SiO₂ layer is deposited and then polished down to 700nm prior to the definition of the cavity. A 10x10 μ m cavity is partially etched at the end of the waveguide leaving roughly 50nm of Si at the bottom of the cavity.

Ge Selective Epitaxial Growth (SEG) in Si cavity

A two-step Reduced-Pressure Chemical Vapor Deposition (RPCVD) process is used to fill the cavity with Ge and accommodate its 4.2% lattice mismatch with Si. First a thin Ge "seed" layer is grown at 400°C, 100 Torr. The remainder of the growth is carried at 750°C, 20 Torr (faster growth rate, smoother surface and defect curing). 3D Atomic Force Microscopy images at various stages of the Ge growth are shown in Fig. 3. Thick, overflowing Ge layers are adopted to avoid faceting inside the cavity. This is also advantageous in terms of Threading Dislocation Density (TDD) which exponentially decreases as the Ge layer thickness increases [5]. The TDD must indeed be as

small as possible since it directly contributes to the dark current density. The SEG is followed by a short thermal cycling under H₂ to further reduce the TDD [6]. Finally a Chemical Mechanical Polishing (CMP) step is used to recover a flat surface and obtain the desired Ge layer thickness. A cross-sectional Transmission Electron Microscopy (TEM) of the resulting stack is shown in Fig. 4.

A SiO₂ layer is deposited prior to ion implantation. A self-alignment process favors a good definition of the doped regions. N-type and p-type regions are implanted with Boron and Phosphorus respectively. Rapid thermal annealing is used to activate the dopants. Contacts on top of the doped Ge regions are fabricated by etching 0.4x0.4 μ m vias which are filled with TiN/W. Electrodes for probing are formed by depositing and patterning Ti/TiN/AlCu metal stack.

3. Results and discussion

Dark current is measured as function of applied bias, with a low value of 25nA under 1V reverse bias as shown in Fig. 5. Photocurrent measurements are carried out with a 1.55 μ m laser source fiber coupled to the photonic circuit using the grating coupler. The maximum responsivity of the photodiode is about 0.5A/W at zero bias, with no dependence on the reverse bias. It means that all photo-generated carriers are effectively collected by the internal built-in electric field. However, the measured responsivity is lower than expected. This can be explained by looking at ion implantation doping profiles. TCAD simulations of ion implantation and thermal annealing process show that the width of the Ge intrinsic region is approximately half of the initial value (Fig. 6), and part of the light is absorbed in the doped region, where carriers are instantaneously recombined. TCAD has been calibrated beforehand thanks to Secondary Ion Mass Spectroscopy (SIMS) profiles of B and P ion implantations in Ge. No further narrowing occurs during annealing as seen from Fig. 7 SIMS profiles.

Theoretical bandwidth is calculated by accounting for RC delay and transit time [7], taking into account the reduction of the intrinsic region width. Maximum -3dB bandwidth is estimated to be over 110GHz and should allow 100Gb/s data rate operation. The measured bandwidth shown in Fig. 8 is limited to 40GHz due to experimental setup limitations. The zero bias bandwidth is measured to be over 40GHz, allowing 40Gb/s and higher data rate operation of the photodiode. Further measurements will be needed to confirm the high predicted value.

4. Conclusions

We reported on the design, fabrication and characterization of waveguide integrated lateral p-i-n Ge on Si photodiodes. A dark current as low as 25nA under -1V bias was measured. The measured bandwidth allows 40 Gb/s operation at zero bias and even faster data rate operation at low bias. Such device can easily be integrated with other photonic devices to fabricate wafer scale photonic integrated circuits for advanced datacom and telecom applications.

Acknowledgements

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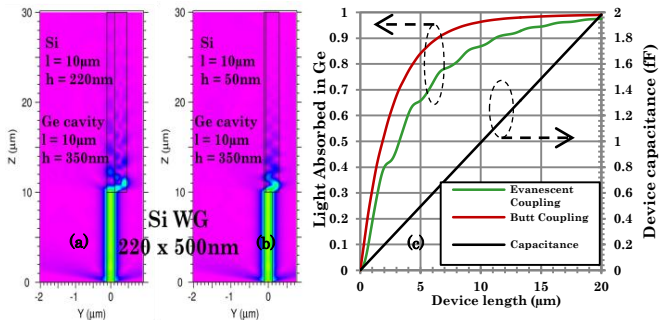


Figure 1. Coupling efficiency and device capacitance. BPM simulation for butt (a) and evanescent (b) coupling configuration. (c) Fraction of light absorbed and capacitance function of the device length for 0.35µm thick Ge layer.

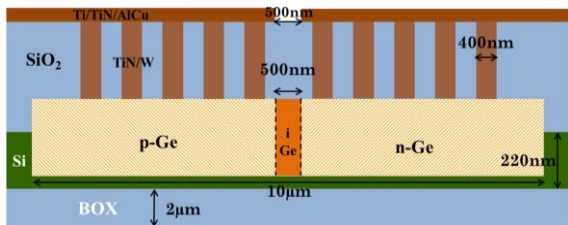


Figure 2. Cross sectional view of the designed waveguide integrated lateral p-i-n photodiode.

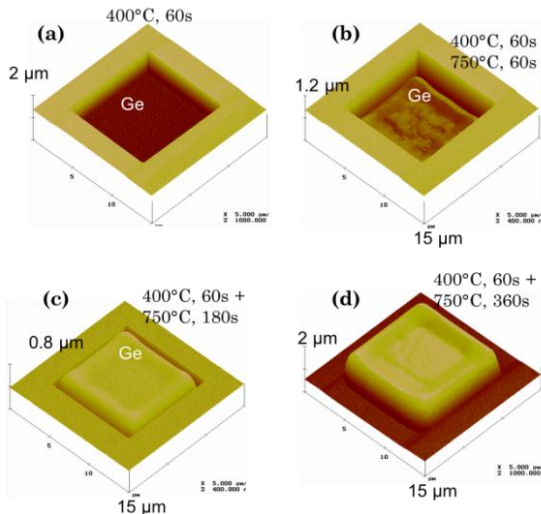


Figure 3. 3D AFM pictures of the Ge SEG inside a 10x10µm cavity. (a) Ge after 60s epitaxy at 400°C. (b) After 60s at 750°C, Ge facets inside cavity visible. (c) After 180s at 750°C, Ge overflowing with facets inside the cavity. (d) After 360s growth at 750°C, cavity fully filled with Ge.

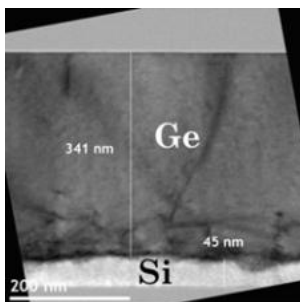


Figure 4. TEM cross section after Ge epitaxy, CMP and oxide encapsulation.

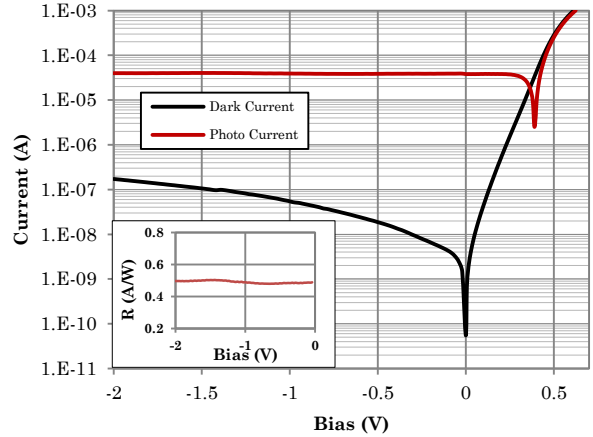


Figure 5. Current versus bias for 10µm long Ge lateral p-i-n photodiode. The responsivity is shown in the inset of the figure.

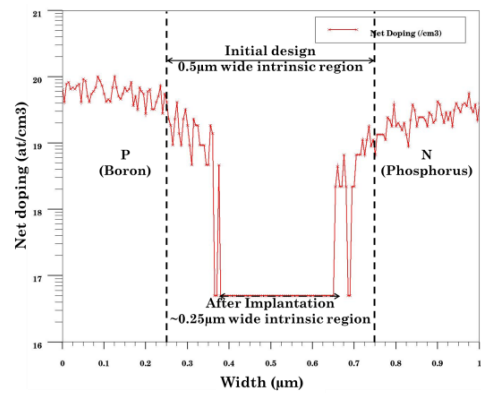


Figure 6. Monte Carlo simulation of ion implantation showing the reduction of the intrinsic region width due to ion implantation.

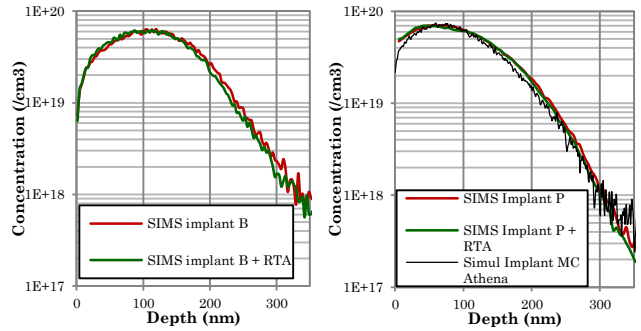


Figure 7. SIMS profile: (a) Phosphorus SIMS profile before and after annealing and Monte Carlo ion implantation simulation. (b) Boron SIMS profiles before and after annealing.

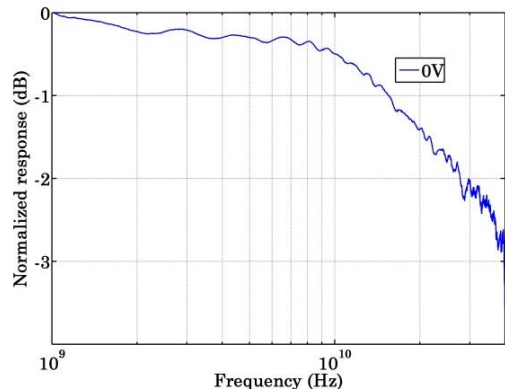


Figure 8. Photodiode frequency response at zero bias.