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An Overview and Future Challenges of High Density DRAM for 20nm and Beyond

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1. Introduction

The dynamic random access memory (DRAM) with one transistor and one capacitor (1T/1C) cell architecture has successfully been scaled down by overcoming lots of scaling challenges [1]. These critical challenges mainly come from the extremely small cell size. In spite of this small cell size, all the components of DRAM should be formed with satisfying the stringent requirements such as sufficient cell charge, small leakage current, and fast charge transfer. However, the DRAM technologies beyond 20nm node will show their fundamental limitations such as patterning, contact process, isolation, and cell capacitor as well as cell transistor [2]. Since technology trends sometimes show not only the rule of the game but also how to break the rule for innovative solutions, it is worthwhile to review and analyze the technology trend at this time.

This paper will be focused on the key technologies of the past generations: cell architecture, lithography, cell transistor, contact, cell capacitor, and bit line technologies. Also, new challenges and approaches will be discussed.

2. Overview and Challenges of Key Technologies

Cell architecture has been evolved from $8F^2$ cell to $6F^2$ cell since the cell size could be reduced up to 75% at the same design rule as shown in Fig. 1. There were a lot of difficulties such as open bit-line noise and challenges from smaller cell size from this change. The difficulties, however, were solved by introducing the low resistance materials, scaling dielectric of storage node capacitor and isolation technologies. The next cell will be $4F^2$, the most effective cell architecture, which needs vertical channel array transistor [VCAT] [3].

In the lithograph, the wavelength of the tool was reduced from 248nm to 193nm. However, the lithography technology has extended to 30nm technology with development of immersion and double patterning technology (DPT). The difference between first and second pattern is a big challenge in DPT for mass product. A great effort to improve the variation of the critical dimension should be one of the most important lithography technologies. Extreme ultraviolet (EUV) lithography tool with 13.5nm wavelength is being prepared for the future as shown in Fig. 2.

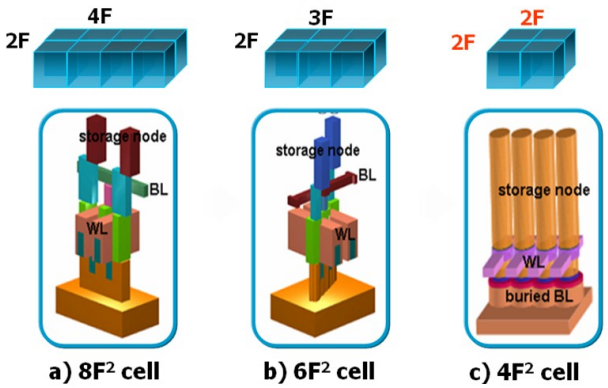

Fig.1 The conceptual and 3D cell architectures show that the cell size has been shrunk at the same design rule (F) from $8F^2$ to $4F^2$ cell.

Cell array transistor has been successfully developed by inventing a recessed cannel array transistor (RCAT) and a buried cannel array transistor (BCAT) up to now. The trend has been increasing the effective channel length in the smaller area. The limitation of the recess type transistor is becoming smaller the width of trench as shown in Fig 3. The small word-line (WL) metal width is worsened by the non-scalable cell gate oxide thickness. To reduce the obstacle, the gate oxide (GOX) scaling technology should be developed. Because VCAT would be free from lateral scaling, it may be one of the best ways to solve the problem even if the silicon pillar resistance may be increased due to

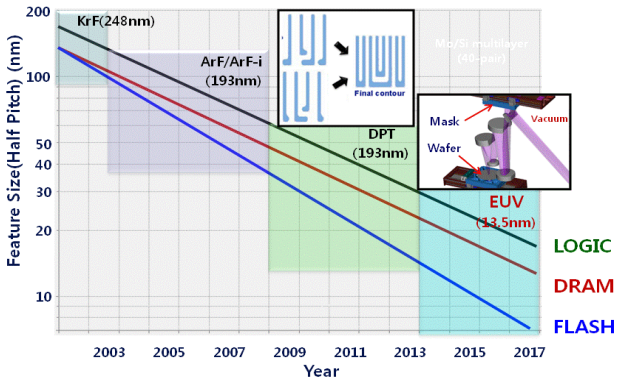

Fig.2 The lithography technologies have been developed. Not only scaling down the wavelength but also using DPT process will be more and more important.

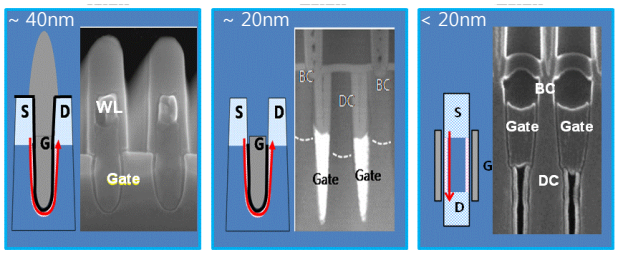

Fig.3 The recess type transistor has been successfully developed. VCAT will be one of the promising solutions beyond 20nm technology.

the small area.

The contact technology has scaled down by self-align method and metallization of the nodes contact. It has two challenges; connection and separation. For the separation, the self-aligned process is essential, even though it is required higher mask height. It should be a big challenge in the bit-line scaling down. For the connection, metallization in the smaller contact size should be a breakthrough technology.

The most critical challenge of DRAM should be a cell capacitor technology because DRAM needs the same cell capacitance in spite of the smaller cell size as previously mentioned. As shown in Fig. 4, the cell capacitor technology has developed in three ways. One is increasing the area of cell. To enlarge the area, there were lots of technologies such as stack/trench cell capacitor, hemispherical grain (HSG) technology, cylinder type storage node, honeycomb type cell layout, and supporter to increase the height without leaning problem. How to keep cylinder type storage node and how to prevent the leaning problem are important in this field. Another is scaling down the dielectric constant of the capacitor material. To scale down the dielectric constant, the higher work function electrode and the higher relative dielectric constant technologies have been rapidly developed for last decade as shown in Fig. 5. The last is reducing the thickness of dielectric. It has scaled down to reach the direct tunneling region. It shows the capacitor

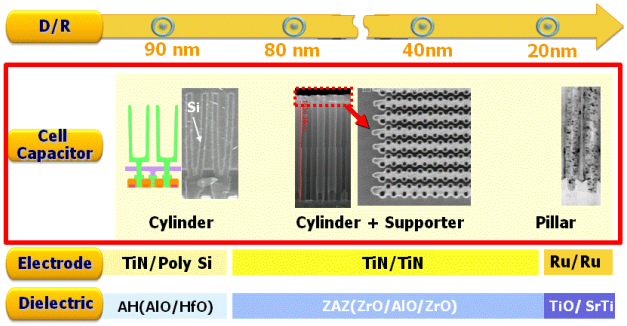

Fig.4 The cylinder type storage node cannot be extended to sub 20nm node due to the thick capacitor dielectric. Not only developing capacitor dielectric but also finding new technology which could increase the area is highly required.

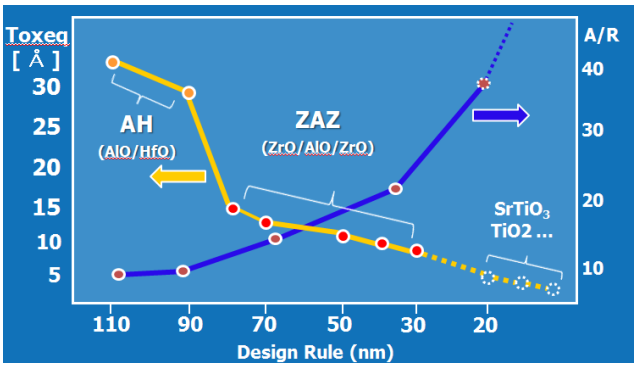

Fig.5 AlO/HfO process was replaced by ZrO/AlO/ZrO process due to the higher dielectric constant. The aspect ratio of storage node will be sharply increased beyond 20nm node.

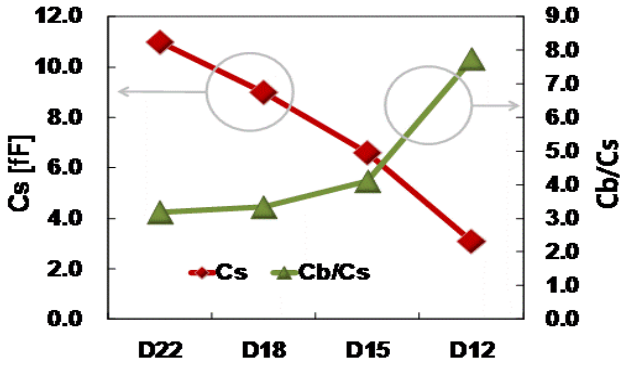

Fig.6 Cell capacitance has been remarkably decreased due to the smaller area and hardly scalable dielectric constant. The bit-line sensing margin will be worse and worse because of increasing Cb/Cs as technology node is smaller.

technology is faced with a limitation in physics in many respects. As a result, cell capacitance (Cs) has been expected to be lower. Thus the ratio of bit-line capacitance (Cb) to Cs has been higher as decreasing the feature size in Fig. 6. The higher Cb/Cs leads the worse the bit-line sensing margin. Reducing Cb is a key technology to overcome this problem. The bit line parasitic capacitance is the best candidate to be handled.

3. Concept of New Approach from Trend

From the overview, we can expect the directions of the technologies in this field. Firstly, it should be required to scale down all the non-scalable factors such as GOX and capacitor dielectric thickness. These non-scalable factors make the small dimension smaller. The word-line resistance will be sharply increased since the metal portion of BCAT will be smaller due to this non-scalable GOX thickness. Secondly, the improvement of electrical characteristics without increasing physical dimension is one of the best ways to solve the scaling issues. Thirdly, the development of self aligned process and the improvement of selectivity of the patterning mask become more and more important in a smaller dimension. Voltage scaling is also mandatory. Finally, it should be essential to develop $4F^2$ cell structure with VCAT in order to achieve bit cost reduction.

4. Conclusions

In this paper, we have reviewed the past DRAM technologies and suggested new technologies to develop in order to overcome some fundamental limitations.

References

[1] Kinam Kim, *International Electron Device Meeting (2005) 323.*

[2] Sungjoo Hong, *International Electron Device Meeting (2010) 292.*

[3] Hyunwoo Chung, et al., *European Solid-State Device Research Conference (2011) 211.*