Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp588-589

Novel Field Effect Diode type Vertical Capacitorless 1T-DRAM Cell with Negative Hold Bit Line Bias Scheme for Improving the Hold Characteristics

Takuya Imamoto[1, 2] and Tetsuo Endoh[1, 2]

[1] Graduate School of Engineering, Tohoku University, [2] JST-CREST
Aramaki aza Aoba 6-6, Aoba-ku, Sendai, 980-8579, Japan
Phone: +81-22-795-4401 E-mail: endoh@riec.tohoku.ac.jp

1. Introduction

Capacitorless 1T-DRAM cell was proposed to overcome the scaling limitations of conventional 1 transistor 1 capacitor DRAM cells [1]. However, 1T-DRAM has short retention time and read disturb problem. Recently, the Field Effect Diode (FED) type 1T-DRAM was proposed [2,3] to achieve low voltage operation and longer retention time. However, this FED type 1T-DRAM needs additional control gate (CG) parallel to Word Line (WL), which causes large cell size, and still have problems on hold characteristics. In this paper, we proposed the novel FED type Vertical capacitorless 1T-DRAM cell with negative hold Bit Line (BL) voltage (V_{BL}). Moreover, we show the improvements of long retention time and BL disturb by comparing with the conventional FED type Planar capacitorless 1T-DRAM through Sentaurus device simulator [4].

2. Proposed Cell Structure and Operation Scheme

Figure 1 (a) and (b) show the cross sectional schematics of the conventional FED type Planar 1T-DRAM (conventional Planar type) and the proposed FED type Vertical 1T-DRAM (proposed Vertical type). The proposed Vertical type is based on the vertical cylindrically pin diode with surrounding gate, CG and non-overlap structure. In the proposed Vertical type, BL, WL, CG, and Source Line (SL) are located vertically and SL and CG is common SL and common CG. Therefore, an ideal cell size of $4F^2$ can be achieved. Table I shows the difference of memory operation scheme between the proposed Vertical type with the conventional Planar type. Figure 2 shows the concept of the proposed Vertical type with negative V_{BL} scheme. In the conventional Planar type, when negative V_{BL} is applied at hold operation, energy barrier of BOX side channel region is lowered due to existence of Back Gate (BG) which is applied to 0V as shown in Fig. 2(a). On the other hand, as shown in Fig. 2(b), the proposed Vertical type can sustain high-energy barrier even when negative V_{BL} is applied at hold operation due to surrounding gate structure and can be achieved excellent hold characteristics.

3. Memory Cell Operation of Proposed 1T-DRAM

Simulated memory cell operation voltages and memory cell design parameters are shown in Table II and III. Undoped channel is assumed, gate work function is set to 4.1eV, and junction offsets are set to 10nm. Figure 3 shows the BL current ($|I_{BL}|$) versus $|V_{BL}|$ characteristics for three different WL voltages (V_{WL}) of the proposed Vertical type. $|V_{BL}|$ is swept by 2V/μsec of the sweep rate. As the $|V_{BL}|$ is increased, $|I_{BL}|$ increases sharply at a point which is determined by V_{WL}. Moreover, $|I_{BL}|$-$|V_{BL}|$ curve shows hysteresis when $|V_{BL}|$ is swept back to 0.0V. Memory operation of the proposed Vertical type at 27°C is shown in Fig. 4. Data can be written and read within 60nsec access time. The current of write "1" and "0" are 4.87μA and 0A. The current of read "1" and "0" are 1.42μA and 6.94pA. In the FED type 1T-DRAM, the current of write "0" is the discharge current of the excess holes in the channel region. Therefore, the current of write "0" is almost zero. From all, it is shown that proposed FED type Vertical capacitorless 1T-DRAM has a good current margin for Write/Read operation.

4. Evaluation of Cell Performances in FED type Planar and Vertical Capacitorless 1T-DRAM

The retention characteristics of the conventional Planar type and the proposed Vertical type are shown in Fig. 5(a) and (b). Each node voltages are set to "Hold" in Table II. The proposed Vertical type shows the retention time of 1,000msec at 85°C, while the conventional Planar type shows the retention time of 1msec. The proposed Vertical type achieved 1,000 times longer retention time than that of the conventional Planar type. BL disturb characteristics of the conventional Planar type and the proposed Vertical type are shown in Fig 6(a) and (b). Each node voltages except for V_{BL} are set to "Hold" and V_{BL} is set to "Read" in Table II. In above bias condition, the proposed Vertical type holds data along 100msec at 85°C, while the conventional Planar type holds along 9μsec. From all, it is shown that the proposed Vertical type achieved about 10^4 times longer BL disturb than that of the conventional Planar type. Summary of the memory cell performances is shown in Table IV.

5. Conclusions

The novel FED type Vertical capacitorless 1T-DRAM cell with negative V_{BL} is proposed and excellent static and disturb retention time are presented for the first time. Proposed Vertical type with negative V_{BL} has the potential to meet DRAM application and extend scaling limitations.

Acknowledgements

This work has been supported in part by a grant from "Research of Innovative Material and Process for Creation of Next-generation Electronics Devices" of CREST under the Japan Science and Technology Agency (JST).

References

[1]T. Osawa, et al., *IEEE J. Solid-State Cir.*, pp. 1510-1522, 2002.
[2]Y. Yang, et al., *Proc. Int. Semicond. Dev. Res. Symp.*, pp. 1-2, 2009.
[3]J. Wan, et al., *IEEE Elec. Dev. Lett.*, pp. 179-181, 2012.
[4] Sentaurus manuals, http://www.synopsys.com Synopsys Inc..

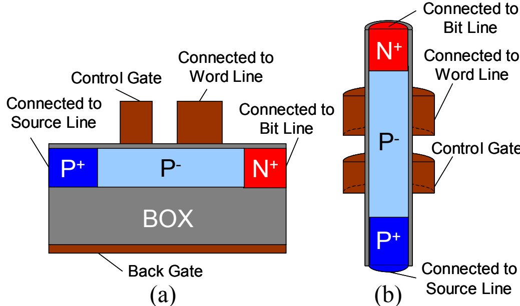


Fig.1 The schematics of the Field Effect Diode (FED) type 1T-DRAM cell.
(a) Conventional Planar type 1T-DRAM cell
(b) Proposed Vertical type 1T-DRAM cell

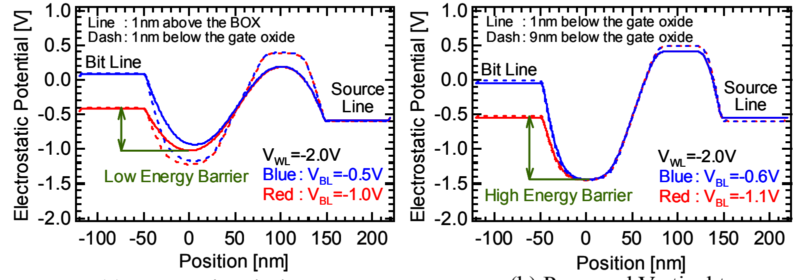


Fig. 2 Concept of novel FED type Vertical 1T-DRAM cell with negative hold Bit Line bias scheme. The proposed Vertical type can sustain high-energy barrier even when negative Bit Line Voltage (V_{BL}) is applied at hold operation, and can be achieve excellent hold characteristics.

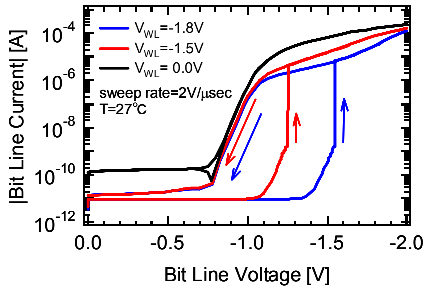
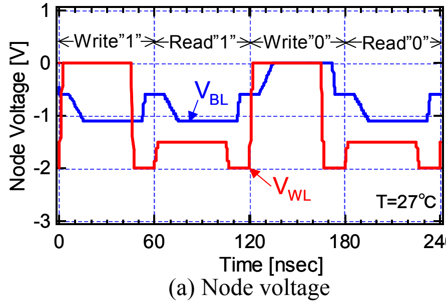


Fig. 3 Bit Line current versus V_{BL} for various Word Line voltages (V_{WL}). Steep and hysterics characteristics are obtained.



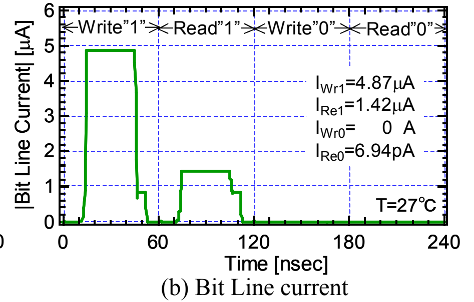
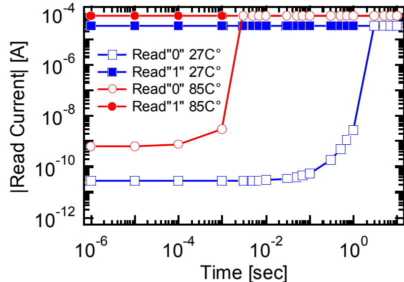
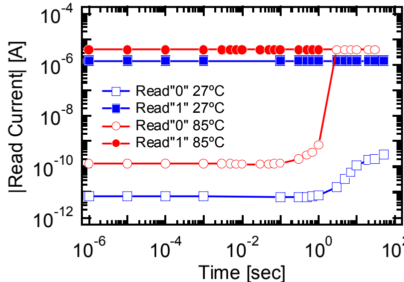


Fig. 4 Memory operation of the proposed FED type Vertical 1T-DRAM cell. Data can be written and read within 60nsec access time. The proposed Vertical type has a good current margin for Write/Read operation.

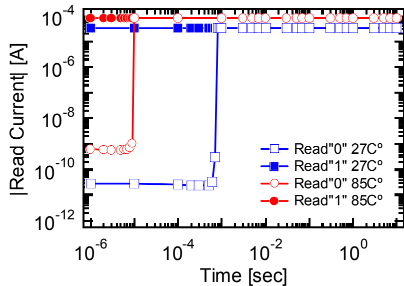


(a) Conventional Planar type

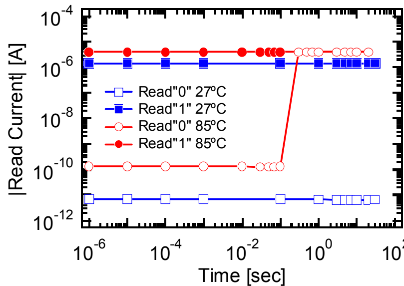


(b) Proposed Vertical type

Fig. 5 Retention characteristics at 27°C and 85°C for the proposed Vertical type and the conventional Planar type. The proposed Vertical type achieved 1,000 times longer retention time than that of the conventional Planar type at 85°C.



(a) Conventional Planar type



(b) Proposed Vertical type

Fig. 6 BL disturb characteristics at 27°C and 85°C for the proposed Vertical type and the conventional Planar type. The proposed Vertical type achieved about 10^4 times longer BL disturb than that of the conventional Planar type at 85°C.

Table IV. Summary of the memory cell performances.

*normalized by (πxD)

	Conventional	Proposed
	Planar type with Zero Hold V_{BL}	Vertical type with Negative Hold V_{BL}
Cell size	**Bad:12F²**	**Good:4F²**
Retention time (85℃)	**Bad:1msec**	**Good:1000msec**
BL disturb (85℃)	**Bad:9μsec**	**Good:100msec**
Read Current (27℃)	**Good:33.5μA/μm**	**Good:22.6μA/μm***

Table I. Difference of memory operations

	Conventional	Proposed
Device Structure	Planar SOI	**Vertical**
Operation Scheme	Field Effect Diode Zero Hold V_{BL}	Field Effect Diode **Negative Hold V_{BL}**

Table II. Memory cell operation voltages

Conv.	Write"0"	Write"1"	Read	Hold
V_{BL}	0.0V	-1.0V	-1.0V	0.0V
V_{WL}	0.0V	0.0V	-1.8V	-2.0V
V_{CG}	0.3V			
V_{SL}	0.0V			
V_{BG}	0.0V			
Prop.	Write"0"	Write"1"	Read	Hold
V_{BL}	0.0V	-1.1V	-1.1V	**-0.6V**
V_{WL}	0.0V	0.0V	-1.5V	-2.0V
V_{CG}	0.3V			
V_{SL}	0.0V			

Prop. Scheme

Table III. Memory cell design parameters

Parameter	Conv.	Prop.
T_{Si}	20nm	
D		20nm
T_{BOX}	140nm	
L_{SP}	50nm	
L_G	60nm	
L_{CG}	50nm	
T_{OX}	5nm	