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Multi-Level Cell Memory with High-Speed, Low-Voltage Writing and High Endurance Using Crystalline In-Ga-Zn Oxide Thin Film Transistor

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1. Introduction

In recent years, a performance gap between nonvolatile memory (NVM) for storage such as flash memory and DRAM used for main memory, has been a problem. In view of the above, various NVMs such as magneto-resistive RAM (MRAM), phase change memory (PCM), resistance RAM (ReRAM) have been proposed; however, these are still under development. Proposed under such circumstances is nonvolatile oxide semiconductor random access memory (NOSRAM) including thin film transistors in which a *c*-axis aligned crystalline oxide semiconductor, In-Ga-Zn Oxide, is used in the channel region (CAAC-IGZO TFTs) [1, 2].

NOSRAM is such highly endurable memory that has unlimited write cycles in principle. Ref. 1 reports that 150 ns/page (1page: 1024bit) writing speed is achieved in 1Mbit NOSRAM. This writing speed is much superior to that of NVMs for storage, which can solve the above problem.

In this work, we discuss the potential of multi-level cell (MLC) aimed at improving memory density of NOSRAM. NOSRAM is charge storage memory and thus, like flash memory, has a possibility of achieving MLC in principle. This is examined using an 8kbit test chip.

2. NOSRAM Cell and its Characteristics

NOSRAM is nonvolatile memory using CAAC-IGZO TFTs having an extremely low leakage current (yocto(10^{-24}) ampere order) [3,4]. Figs. 1(a) to (d) show a circuit diagram and basic characteristics of the NOSRAM cell. As shown in Fig. 1(a), the NOSRAM cell includes a data writing IGZO TFT, a data reading PMOS, and a cell capacitor C for charge storage and controlling PMOS gate voltage. In writing data, a write word line (WL_{IGZO}) is set to "High" so that the IGZO TFT is turned on, and the cell capacitor C is charged and discharged through the IGZO TFT from a bit line (BL). When the WL_{IGZO} is set to "Low", the stored charge is expected to be retained for a long time due to the extremely low leakage characteristic of the IGZO TFT. In reading data, a difference in threshold voltage (*V*th) of a memory cell depending on stored charge is utilized. Data is identified by controlling on/off of the data reading PMOS, using a write and read word line (WL_C). Figs. 1(b), (c) and (d) respectively show the current characteristics, the write endurance and the relation between writing time and ΔVth of the NOSRAM cell. These figures indicate a shift in the current characteristics corresponding to data (Fig. 1(b)), high write endurance of more than 10^{12} cycles (Fig. 1(c)) and that data can be written at 10 ns (Fig. 1(d)).

Here, the possibility of achieving MLC NOSRAM is considered. In MLC Flash memory, the verify operation is performed; it takes time to write data. On the other hand, in NOSRAM, a potential can be directly supplied to a memory cell, whereby the amount of the stored charge can be precisely controlled. Thus, *V*th distribution after the writing is expected to have a sharp peak without performing the verify operation, therefore, NOSRAM is suitable for MLC.

3. Results and Discussion

Fig. 2 shows an 8kbit test chip fabricated in 0.8 μm process technology. In a memory cell, IGZO TFT W/L = 1.4 μm/1.2 μm; PMOS W/L = 0.8 μm/0.8 μm; and C = 2 fF. The memory cells are arranged in 512 rows and 16 columns.

Fig. 3 shows measured 4-level *V*th distribution. The data has 4-levels of "*A*", "*B*", "*C*" and "*D*" at 0 V, 1.6 V, 2.1 V and 3 V, respectively. In the figure, initial *V*th distribution and that after 10^8 write cycles are described. Table I shows the calculated values of μ and 3σ (μ: average value, σ: standard deviation) of each peak. As expected, the *V*th distribution had a sharp peak, and 3σ was approximately 120 mV. Note that in the test chip, the memory cells were arranged only in 16 columns, so that variation due to a reading circuit is suppressed, and intrinsic *V*th distribution of the memory cell can be estimated. The possibility of 4-level cell (2b/cell) NOSRAM capable of writing at high speed (without the verify operation) can be confirmed. Fig. 3 and Table I show that the *V*th distribution does not change even after 10^8 write cycles. Fig. 4 shows data retention characteristics (85 °C) at the time of data writing "*D*". In Fig. 4(a), *V*th distributions at respective times are each plotted. Fig 4 (b) shows time dependence of average value μ in the measured *V*th distribution. After 180 hours, the peak shifted by about 110 mV. From this result, the period of data retention at 85 °C is estimated to about 23 days assuming that a margin between states is 250 mV. An improvement in the data retention is an issue in the future.

4. Conclusions

The possibility of achieving multi-level cell NOSRAM, nonvolatile memory including CAAC-IGZO TFTs, was examined. The 8kbit test chip exhibited a sharp *V*th distribution of 3σ of approximately 120 mV, which means the possibility of 2b/cell NOSRAM. Further, with the chip, write endurance of 10^8 cycles and data retention at 85 °C for about 23 days are confirmed. These results indicate the possibility of achieving a nonvolatile memory with high memory density as well as high-speed, low-voltage writing and high endurance.

References

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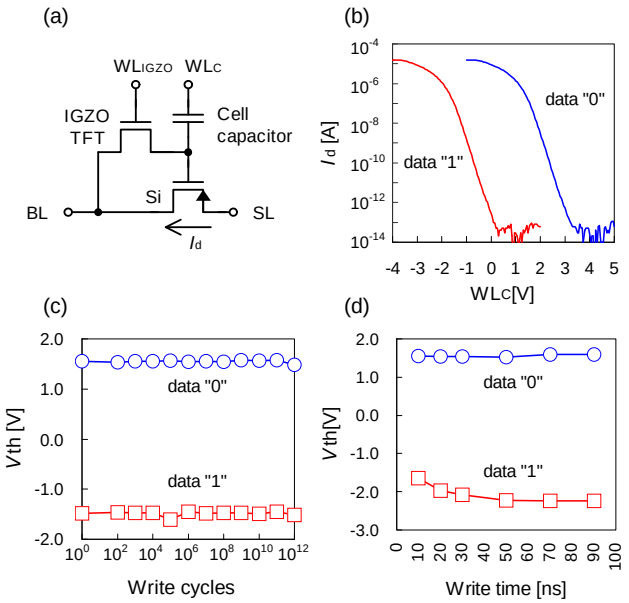

Fig. 1 Basic characteristics of NOSRAM cell. (a) Circuit diagram. (b) Current characteristics. (c) Write endurance. (d) Relation between writing time and ΔVth.

Table I Calculated values of μ and 3σ with respect to *V*th distribution (Fig. 3).

	Initial		After 10^8 cycled	
	μ [V]	3σ [mV]	μ [V]	3σ [mV]
A	0.863	85.8	0.857	83.1
B	1.56	142	1.54	144
C	2.13	126	2.11	131
D	2.87	106	2.85	109

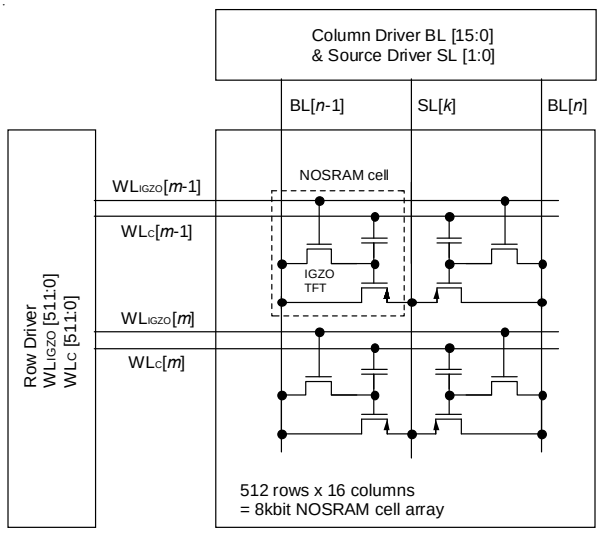

Fig. 2 Block diagram of 8kbit test chip.

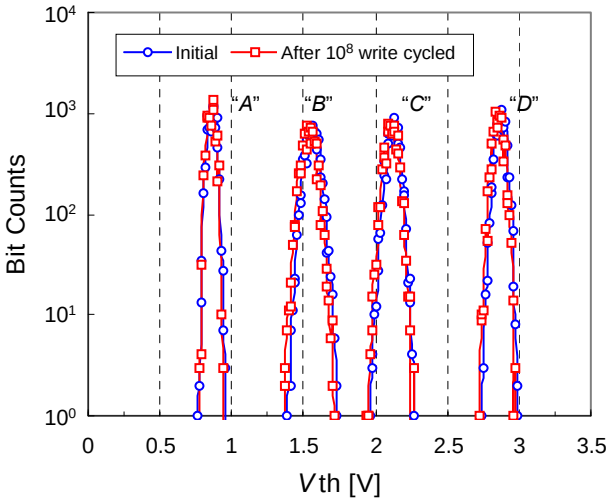

Fig. 3 Measurement of 4-level *V*th distribution.

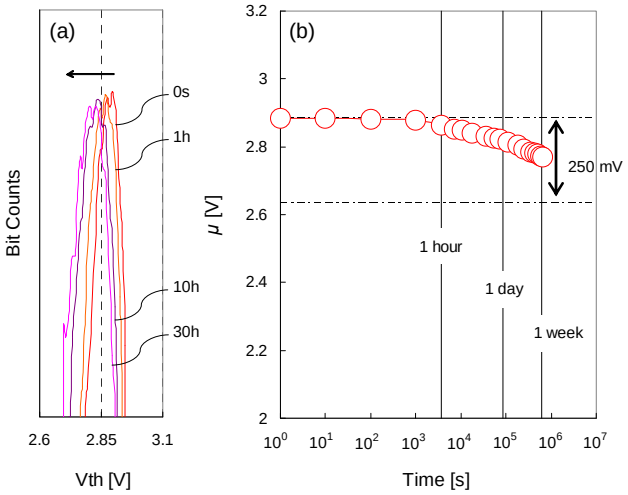

Fig. 4 Data retention characteristic at 85 °C. (a) Distribution in writing data "*D*". (b) Change in μ with time.