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# Characterization RTN(Random Telegraph Noise) Generated by Process and Cycling Stress Induced Traps in 26 nm NAND Flash Memory

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## 1. Introduction

Recently, NAND flash memory has been widely used as a mass data storage device and the size of data has increased. In order to meet ever increasing market demand of storage capacity, aggressive efforts for scaling NAND flash devices have been made and the cell size in planar channel NAND flash memory has been scaled down to 15 nm node [1]. As the result of the scaling-down, NAND flash memory has been faced with various problems such as read disturbance, cell-to-cell interference, program saturation issue, and so on [2]-[4]. Among these problems, RTN which is caused by the capture/emission of an electron at a trap inside tunneling oxide becomes one of the critical issues, because increasing bit-line (BL) current fluctuation ($\Delta I_{BL}$) with scaling-down of cell size can make an error during read operation and the memory unreliable. Especially, the trap which is responsible for RTN can be not only generated during fabrication process but also generated by cycling stress. However, no report has been made on the characterization of instability by RTN generated by the cycling stress.

In a previous paper [5], a methodology to extract the 3-D position of trap generated by process was introduced. In this work, we investigate systematically RTN generated by process and cycling stress induced traps.

## 2. Device Structure and Result

In this work, we characterized NAND flash cell strings fabricated with 26 nm technology. It consists of sixty-four cells, two dummy cells, a drain select line (DSL) transistor and a source select line (SSL) transistor. The channel length and width are 26 nm and 20 nm, respectively.

To check RTN generated by cycling stress induced trap, first, we measured the BL current ($I_{BL}$) in time domain and normalized noise power spectral density ($S_I/I_{BL}^2$). Here, $I_{BL}$ is 100 nA when bit-line voltage ($V_{BL}$) and pass voltage ($V_{PASS}$) are 0.8 and 6.5, respectively. Then we measured $I_{BL}$ and $S_I/I_{BL}^2$ at same bias condition after 1000$^{th}$ and 2000$^{th}$ cycling.

Fig. 1 (a) and (b) show $I_{BL}$ of a cell before cycling and after 2000$^{th}$ cycling, respectively, in the time domain. Before the cycling stress, RTN was not observed. After 2000$^{th}$ cycling stress, RTN was generated and $\Delta I_{BL}$ was ~70 nA. In another cell as shown in Fig. 1 (c), we can observe small RTN before cycling, which means the trap was generated during fabrication process. In this figure, relatively fast and small RTN ($\Delta I_{BL}$ = 4.5 nA) is observed. After cycling the cell by 2000$^{th}$, slow and large RTN ($\Delta I_{BL}$ = 40 nA) is generated in the cell as shown in Fig. 1 (d).

Fig. 2 (a) and (b) show $S_I/I_{BL}^2$ corresponding to $I_{BL}$ fluctuations of two different devices: (a)-(b) and (c)-(d) in Fig. 1, respectively. In Fig. 2 (a), $S_I/I_{BL}^2$ is increased significantly (more than several hundred times in the frequency range from 10 Hz to 2 kHz) by a cycling stress induced trap. Below 100 Hz, $S_I/I_{BL}^2$ after cycling is larger than that before cycling as shown in Fig. 2 (b). However, in the frequency range higher than 100 Hz, $S_I/I_{BL}^2$ of the device after cycling shows lower since the fresh device has a fast changing RTN with small amplitude.

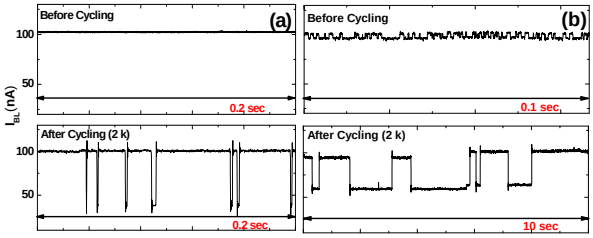


Fig. 1. Bit-line current fluctuation ($\Delta I_{BL}$) in time domain before and after cycling stresses. (a)-(b) RTN is generated after 2k cycling. (c)-(d) Multi-level RTN is generated after 2k cycling.

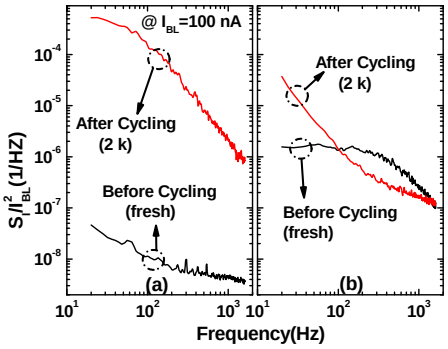


Fig. 2. Normalized noise power spectra corresponding to $I_{BL}$ fluctuations in Fig. 1 (a)-(b) and (c)-(d).

To obtain more reliable information on the cycling stress, cumulative probability of $S_I/I_{BL}^2$ at 20 Hz and $\Delta I_{BL}$ are prepared in Fig. 3. These data were measured in several hundred devices at $I_{BL}$ of 100 nA. Square symbols represent measured data in the fresh devices. The data represented by solid circles are obtained after 1000$^{th}$ cycling. The data after 2000$^{th}$ cycling are represented by triangle symbols. As the number of cycle increases, $S_I/I_{BL}^2$ and $\Delta I_{BL}$ are increased. In the fresh devices, the distribution of $S_I/I_{BL}^2$ ranges from $3\times10^{-8}$ to $5\times10^{-5}$, and the range is increased from $10^{-7}$ to $5\times10^{-4}$ after 2000$^{th}$ cycling. Especially, $\Delta I_{BL}$ was increased up to 80 nA which is 80% of a read current

of 100 nA after 2000th cycling. The more you cycle NAND flash memory cells, the larger fluctuation will be happened.

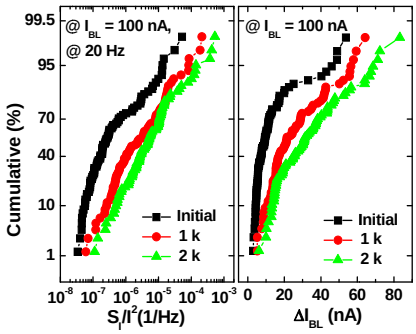


Fig. 3. Cumulative probability of noise power spectral densities at 20 Hz and $\Delta I_{BL}$ with cycling stress. Here, $I_{BL}$ is fixed at 100 nA.

Then we study the position of traps responsible for RTN in x-y plane, because the effect of traps is quite different with the position of traps. We extracted the position of traps ($x_T$: a trap position within the tunneling oxide from the channel surface, $y_T$: a trap position within tunneling oxide along the channel length direction) by using the method in [5]. In extracting the position of traps, channel resistance effect except that of a read cell should be considered because a cell string consists of sixty-four unit cells, two dummy cells, and two select transistors (a DSL and a SSL). The measured devices have a tunneling oxide thickness of 7.9 nm. Fig. 4 shows the extracted $x_T$ and $y_T$ for process induced traps in 30 cells. We understand the traps are roughly located around both edges of the channel, which seems to be come from the gate etch process [6].

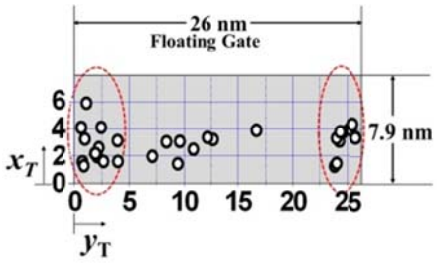


Fig. 4 Extracted vertical ($x_T$) and lateral ($y_T$) trap positions of process induced traps in the tunneling oxide.

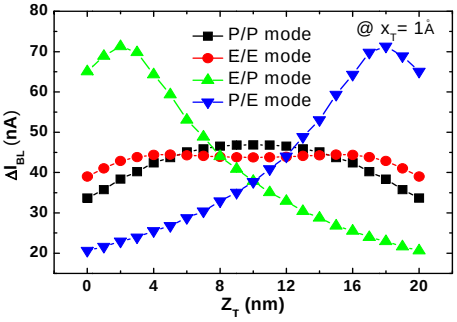


Fig. 5. Simulated $\Delta I_{BL}$ with a trap position along the channel width ($z_T$) as a parameter of the state (program or erase) of adjacent BL cells when the trap depth ($x_T$) is 1 Å.

In order to extract a trap position along the channel width direction ($z_T$), we also use the method in [5]. In Fig. 5, the change of simulated $\Delta I_{BL}$ with the $z_T$ as a parameter of the state (program or erase) of adjacent BL cells was shown when the $x_T$ in the tunneling oxide is 1Å. The bias condition used in this simulation is exactly the same as above ($I_{BL}$ = 100 nA, $V_{BL}$ = 0.8 V and $V_{PASS}$ =6.5 V). Simulated $\Delta I_{BL}$s are shown along the channel width direction with the state of adjacent BL cells. For example, if $\Delta I_{BL}$ is 70 nA, the high level current is 100 nA and the low level current is 30 nA. And P/P mode means that adjacent cells are both programmed ($V_{th}$ = 3 V). The $V_{th}$ of a read cell is set to 0 V. In E/E mode, both adjacent BL cells are erased ($V_{th}$ = -3 V). Based on the behavior of $\Delta I_{BL}$ with the state of adjacent BL cells, we can extract the position of $z_T$. Finally, Fig. 6 shows the 3-D position ($x_T$, $y_T$, and $z_T$) of extracted traps after cycling stress. Big symbols represent the 3-D position of traps within the tunneling oxide. Small symbols stand for the trap position projected on y-z, x-z, and x-y planes. According to 7 traps extracted, the position of the traps generated by the cycling seems to be random in the tunneling oxide and need further research with more cells.

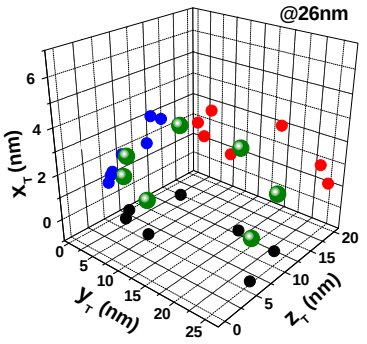


Fig. 6. Extracted $x_T$, $y_T$ and $z_T$ of cycling stress induced traps in the tunneling oxide. Small symbols are trap position projected on each plane.

## 3. Conclusions

In this paper, we have investigated key properties of RTNs from process and cycling stress induced traps through 3-D device simulation and measurement in 26 nm NAND flash memory. It was shown that read current fluctuation and noise power were increased significantly with cycling stress induced trap. 3-D trap position of stress induced traps were successfully extracted.


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