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Single-Poly Flash Memory with Degradation-Separated Scheme

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1. Abstracts

The embedded NVM technologies have been widely applied to logic-compatible processes [1] [2] for growing SOC demands, such as SMART CARD or NFC fields. A new NVM cell fully compatible with conventional logic process is introduced. Such a memory cell is fabricated by a typical 3.3V process, without any additional process steps or process change. Good characteristics are verified by using of both a single-cell testkey and a 1kbits test-array, demonstrating the feasibility of itself as an embedded NVM solution. Excellent endurance over 100K cycles is demonstrated and good retention result after 100K cycles have been presented as well.

2. Cell structure and its operation

The proposed new cell is composed of four transistors and one capacitor, as in the Fig.1 to implement a single-poly floating-gate non-volatile memory device. The floating gate is shared by one n-MOSFET (M_{N1}), one p-MOSFET (M_{P1}) and one coupling capacitor (C_1); while the drain of M_{N1} connects to a read terminal, the drain of M_{P1} connects to a programming one. M_{N1} and M_{P1} are connected to their select-transistors, M_{N2} and M_{P2}, individually. As indicated in Fig. 1, the coupling capacitor, the two n-MOSFETs, and the two p-MOSFETs are enclosed with respective n-wells and p-well.

Table 1 suggests the operation schemes for the new cell. The program and erase operations are performed on p-MOSFET by channel hot hole induced hot electron injection [3], and electron channel Fowler-Nordheim tunneling ejection, respectively. The read operation is performed on n-MOSFET by sensing read conduction current. Unlike conventional NVM devices, the proposed cell operation separates read path from program and erase path, in order to reduce the impact of program/erase operation induced degradation, such as Vth-window closure due to possible charge residues on gate dielectric layer. Therefore, an enhanced read current window is obtained for high reliability operation.

3. Characterization Results and Discussion

Figure 2 shows the programming and erasing characteristics. By using of hot carrier injection at p-channel M_{P1}, the cell can be easily programmed with 6V in 100us; while a properly selected erasing bias applied (between 8 to 9V), the cell can be erased completely within 100ms. Fig. 3 shows the endurance trend by reading from n-channel M_{N1}. Vth-window is still good for read even after 10^6 program/erase cycles. Compared to read from p-channel M_{P1}, Vth-window by reading from M_{N1} has less degradation due to program/erase cycling stress as shown in Fig. 4. Fig. 5 and 6 illustrate the ID-VG characteristics of M_{N1} and M_{P1} before/after 10^6 program/erase cycles. Only Vth shift is observed for M_{N1} after program/erase cycle stress, which may come from the electron residue in floating-gate due to the degraded program/erase ability. For ID-VG curves of M_{P1} in Fig. 6, except for the electron residue, obvious sub-threshold swing degradation (20%) is observed, which indicates the operation-induced interface states change on M_{P1} after 10^6 program/erase cycling stress. Fig. 7 further depicts the energy-band diagrams of M_{P1} with gate oxide damages and the corresponding degradation mechanism. Electron trapped in gate-oxide lowers the electric field and causes inefficient FN-tunneling erasure, and then result in electron residues in floating-gate. The interface state generation caused by the impact of hot electron injection results in mobility degradation and subsequent degraded channel hot carrier injection.

Figure 8 shows retention characteristics of program and erase state, regarding fresh, 10K-cycled and 1M-cycled cells. No significant Vth-window degradation is observed even after 250C, 100hr baking.

Figure 9 and 10 further present program and erase state read current window and current distribution of a 1k-bit array during 100K cycling and excellent 1k-bit array retention after 250C 150hr baking.

4. Conclusion

A promising 100% logic compatible NVM cell array for high reliability application is successfully demonstrated. With separate PGM-READ-path-design, the proposed cell structure provides large operation window and reliability window only with insignificant degradation even after 10^6 program/erase cycling stress. A simple mechanism is proposed to explain the observed degradation phenomena and why separate PGM-READ-path-design realizes good design window.

Reference

[1] K. Yoshikawa et. al., TED, Vol. 37. No.3, p.675, 1990
[2] K. Ohsaki et. al., JSSC, Vol. 29, NO. 3, p.311, 1994
[3] C. C.-H. Hsu et. al., SSDM, p.140, 1992

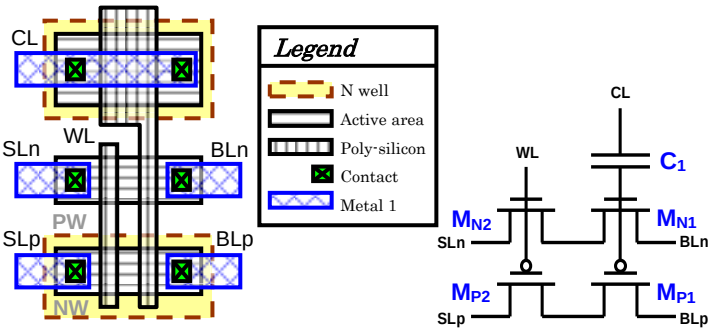

Fig. 1 The proposed cell is composed of three staggered well implant regions, defining p-FETs as PGM & ERS channel, and n-FETs as read channel

	CL	WL	SLn	BLn	SLp	BLp
PGM	5.5	5.0	0.0	0.0	6.5	0.0
ERS	0.0	3.3	0.0	0.0	8.5	8.5
Read	1.8	1.8	0.0	1.5	1.8	1.8

Table 1 The suggestion operation schemes with separate READ path and PGM/ERS path to reduce the impact of Vth-window closure

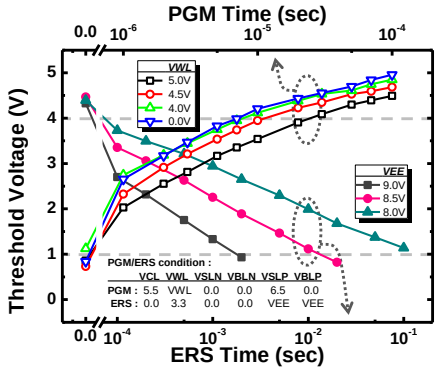

Fig. 2 The characteristics of programming by hot carrier injection and erasing by Fowler-Nordheim tunneling

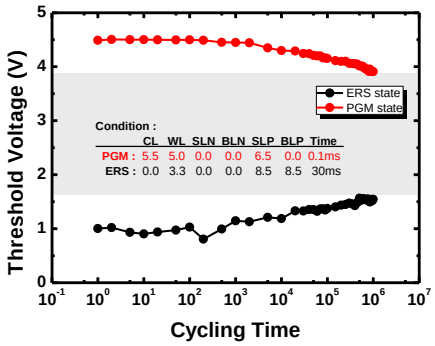

Fig. 3 The endurance trend read from n-channel under typical bias condition and temperature with sufficient Vth-window after 1M cycles test

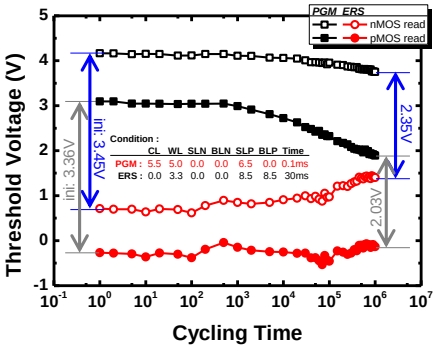

Fig. 4 The comparison of Vth endurance trend between n- / p- channel read

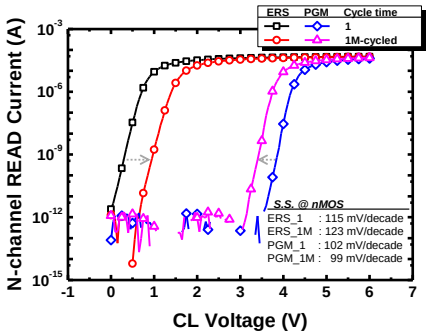

Fig. 5 The n-FET ID-VG curves between 1 & 1M cycled times at both PGM- / ERS- states.

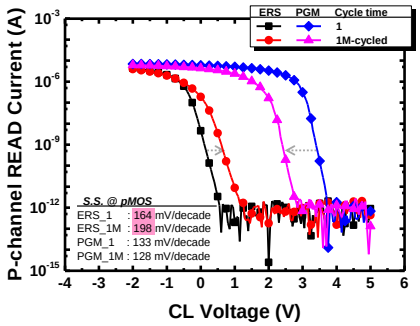

Fig. 6 The p-FET ID-VG curves between 1 & 1M cycled times at both PGM- / ERS- states.

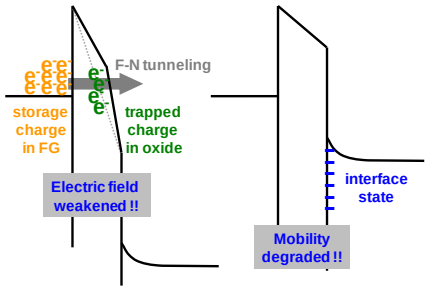

Fig. 7 The energy band diagram to illustrate the gate oxide damage of p-FET (M_{P1}) after 1M cycled-times.

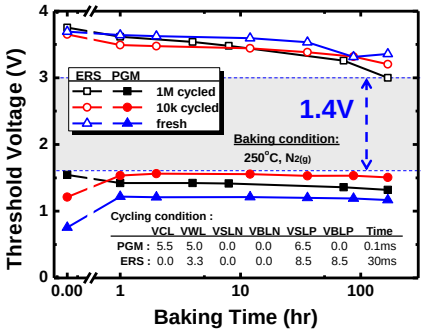

Fig. 8 Retention baking trends of programmed and erased state, regarding fresh cells, 10K-cycled and 1M-cycled cells

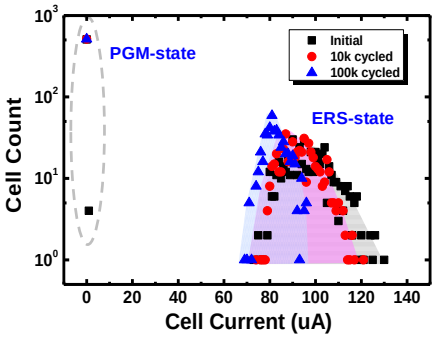

Fig. 9 ON- and OFF-state current window of a 1k-bits array, and the trend of cell current distribution during 100k cycling respectively

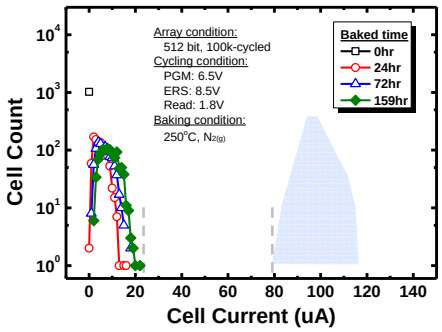

Fig. 10 The characteristics of charge retention after 100K cycling-times