Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp600-601

B-2-5L

Exploring Trapped Charge Evolution in P-Channel SONOS Memory Device

Fu-Hai Li[1,*], Yung-Yueh Chiu[1], Yen-Hui Lee[1], Ru-Wei Chang[1], Bo-Jun Yang[1], Wein-Town Sun[3], Eric Lee[3] and Chao-Wei Kuo[3], Riichiro Shirota[1,2]

[1]Institute of Communications Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[2]Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[3]SONOS Technology Research Program, eMemory Technology Inc. Jhubei City, Hsinchu 302, Taiwan
[*]Corresponding author: TEL: +886-3-5712121 ext: 31704, Email: pilee.eo94@nctu.edu.tw

Abstract. The charge distribution in SiN layer by dynamic programming (PGM) of Channel Hot Hole Induced Hot Electron injection (CHHIHE) is precisely investigated in p-channel SONOS memory device. 3D device simulation is calibrated by comparing the measured programming characteristics. It is found, for the first time, that the hot electron injection point quickly traverses from drain to source side synchronizing to the expansion of charged area in SiN layer. The injected charges quickly spread over on the almost whole channel area uniformly during a short dynamic PGM period, which will afford large tolerance against lateral trapped charge diffusion by baking. This characteristic is different from the case of n-channel SONOS, where injected charges are locally concentrated near to drain side.

1. Introduction

Many studies have been done for charge localization during program in n-channel SONOS devices [1, 2]. Recently, in order to achieve high performance and highly reliable embedded Flash memory, lot of interest has been focused on p-channel SONOS memory devices [3, 4]. Hot electron injection efficiency in p-channel devices can be higher than that in n-channel devices [5]. Furthermore, the hot-hole-free operation scheme in p-channel device further reinforces the reliability [6]. Dynamic PGM scheme with gate voltage step up pulses has been proposed [7] to achieve higher programming efficiency and low bit-line bias operation. However, the trapped charge distribution induced by CHHIHE in p-channel SONOS device has not been explored yet. In this paper, we explore the dependence on the programming time of trapped charge distribution with various pulse width and number of pulses.

2. Experiment and simulation results

The p-channel SONOS devices under analysis are presented on Fig.1-a. The trapped charge density (T_D) and the effective trapped charged length (T_L) are extracted [1], as shown in Fig.1-b. Fig.1-c shows the programming window of ΔVt_R (i.e., the difference between Vt in reverse read (RR) and the initial state Vt) and ΔVt_{RF} (i.e., the reverse to forward Vt difference). Fig.1-d and Fig.1-e show the bias setting and the programming waveform of dynamic PGM method [4]. The increment gate voltage step up pulse is used with 7 steps as shown in Fig. 1(e) and 3 kinds of pulse width (1μs, 7μs and 14μs) are examined. Initial state before programming is prepared by FN-erasing and electrons are uniformly distributed ($9.5\times10^{18}cm^{-3}$) in SiN as shown in Fig.1-f. The simulated n- and p-channel contour plot of ΔVt_R and ΔVt_{RF} as a function of T_L and T_D are exhibited in Fig.2-a, Fig.2-b, Fig.3-a and Fig.3-b. In the case of n-channel device, charges in SiN locally concentrate near to drain side to get ΔVt_{RF} more than 1V, as shown in Fig.2-b [1]. However, in the case of p-channel device, charges in SiN need to be extended into source side to get ΔVt_{RF} more than 1V, as shown in Fig.3-b. This difference comes from the formation of local inversion layer in the p-channel device when electrons are injected in SiN layer. Fig.3-c and Fig.3-d are simulated channel surface potential associated with case1~4 as marked in Fig.3-a, where different T_L and T_D are placed. The equivalent value of ΔVt_R is observed between case 1 and 2 or between case 3 and 4. In comparison of case1 and case2, the maximum potential barrier heights are the same even though they have the different T_D. On the other hand, in comparison of case3 and case4, the potential barrier heights also are the same in spite of the different T_L. Fig.4-a and Fig.4-b show the measured ΔVt_R and ΔVt_{RF} as a function of gate voltage step up pulse. It indicates that pulse width 7μs have the best PGM efficiency. Fig.4-c shows ΔVt_R versus ΔVt_F (the difference between Vt in forward read and the initial state Vt) for the analysis of charge uniformity. After PGM time longer, ΔVt_R v.s. ΔVt_F curves approach the line ($\Delta Vt_R = \Delta Vt_F$) in both of pulses width 7μs and 14μs. It means the charges are getting uniformly distributed in SiN as program step number increased. Fig.5-a shows the simulated trapped charge evolution curve dependent on program step number, coupled to the measured results. Between two pulses width (7μs and 14μs), T_L and T_D have the same trajectory, even though they have the different PGM speed. Consequently, it is shown that the trapped charge smoothly extends into the SiN layer in 7 program steps. The Electric field associated with different T_L during PGM period is shown in Fig.5-b. The accumulated trapped charges in SiN layer and the pinches-off point below the channel will move from drain side toward source side. Fig.5-c shows the measured and simulated PGM window in forward and reverse read with various pulse widths. The measured and simulated I-V curves show good agreements. In n-channel device, the Vt is sensitive to T_L. However, in p-channel device, the charge almost uniformly distributed into SiN and the Vt is insensitive to T_L. Therefore, by using FN erase plus CHHIHE PGM, uniform charge transfer between n-substrate and SiN layer is executed, which will ensure the robust program and erase operation.

3. Conclusions

In this paper, we have quantitatively traced the evolutionary trapped charge distribution induced by various dynamic pulse times in p-channel SONOS device. During a short dynamic PGM period, the trapped charges quickly extend into the SiN layer of the whole p-channel based on our result. On the other hand, the channel length self-modulation can reduce the PGM stress of gate oxide. This study provides a comprehensive understanding and design guidelines for p-channel SONOS devices.

Acknowledgements

The authors would like to thank Chun-Yuan Lo, Chia-Jung Hsu and all members of SONOS Technology Research Team of eMemory Technology Inc., Taiwan for the preparation of the samples and supports of characterization.

References

[1] Luca Perniola et al., IEEE TNANO, 4, p.360, (2005).
[2] Etienne Nowak et al., SSDM Tech. Dig., p. 152, (2009).
[3] HM Lee et al., SSDM. Tech. Dig., p. 196, (2005).
[4] Wein-Town Sun et al., ICICDT Tech. Dig., #F-3 (2011).
[5] C.Hu, VLSI Tech, Dig., p.119, (1989).
[6] K.Ng et al., IEEE TED,p.871, (1983).
[7] Y. J. Chen et al., IRPS , p. 824-827 (2011).

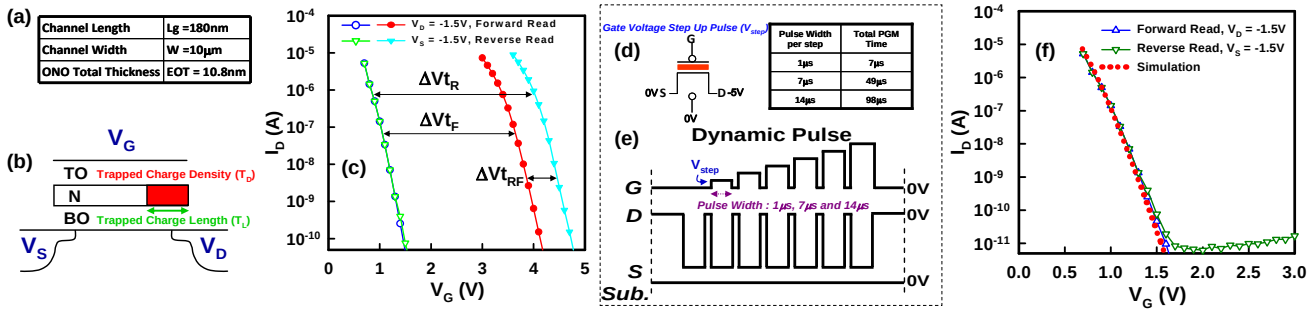

Fig. 1. (a) Parameter of the p-channel SONOS device under analysis. (b) The trapped charge density (T_D) and the effective trapped charged length (T_L) are extracted.(c) ΔVt_R and ΔVt_F is the programming window in reverse and forward read condition. ΔVt_{RF} is the reverse to forward Vt difference. (d) and (e) Bias setting , PGM waveforms with various pulses used in this work (f) Comparison of the measured and simulated I-V with forward and reverse read for initial state.

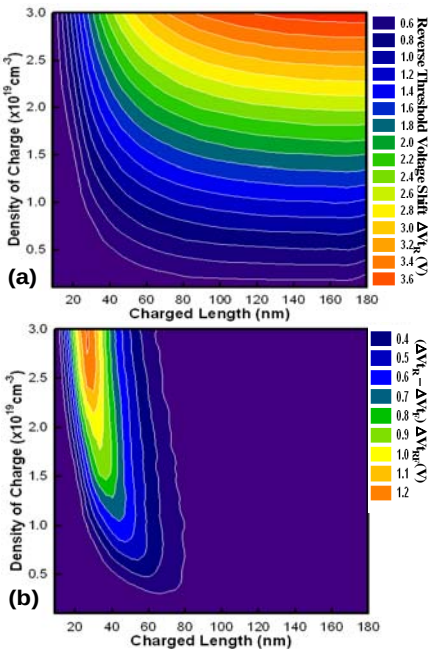

Fig. 2. N-channel contour plots of (a) ΔVt_R and (b) ΔVt_{RF} as a function of T_L and T_D.

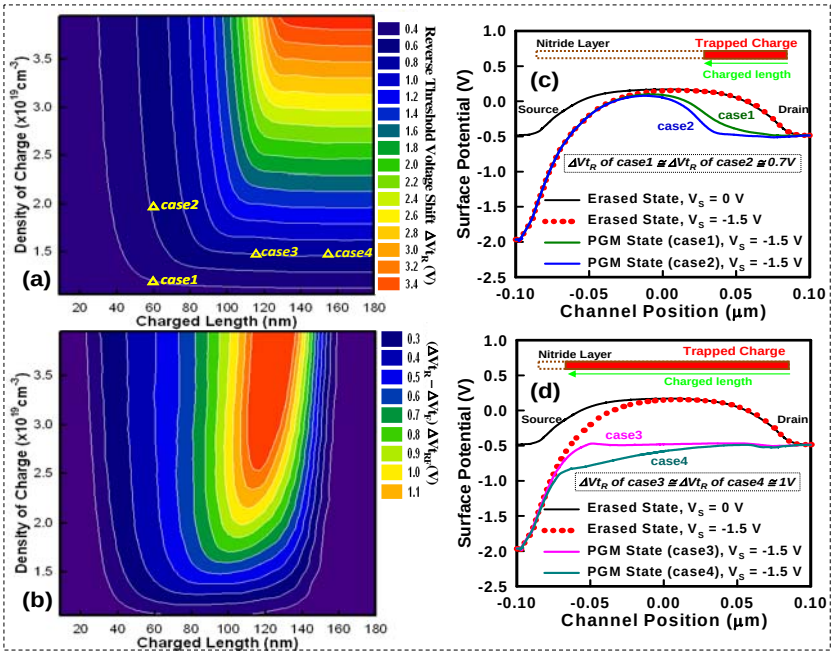

Fig. 3. P-channel contour plots of (a) ΔVt_R and (b) ΔVt_{RF} as a function of T_L and T_D. (c) and (d) simulated channel surface potential associated with (case1~4 as marked in (a)) .

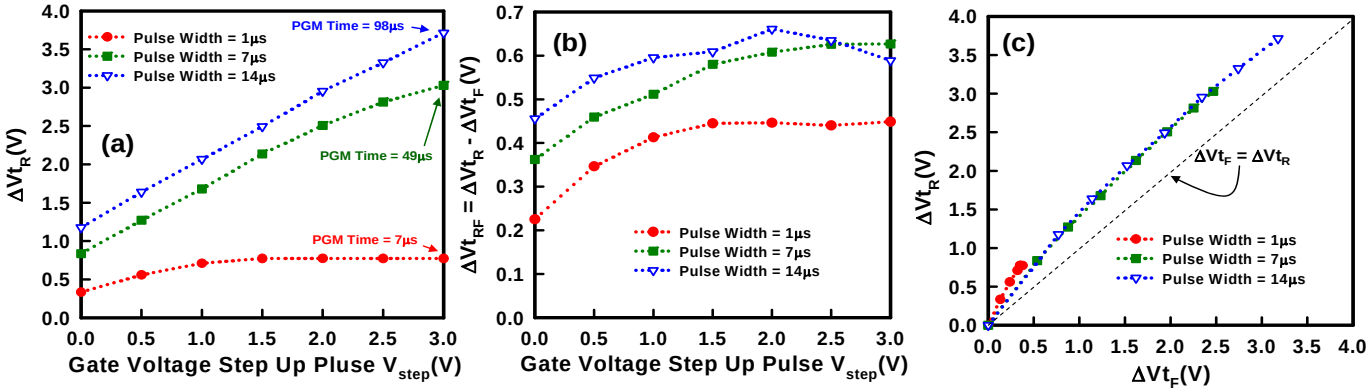

Fig. 4. Measured (a) ΔVt_R and (b) ΔVt_{RF} as a function of gate voltage step up pulse.(c) ΔVt_F versus ΔVt_R for the analysis of charge uniformity resulting from various pulse widths, such as 1us, 7us and 14us respectively.

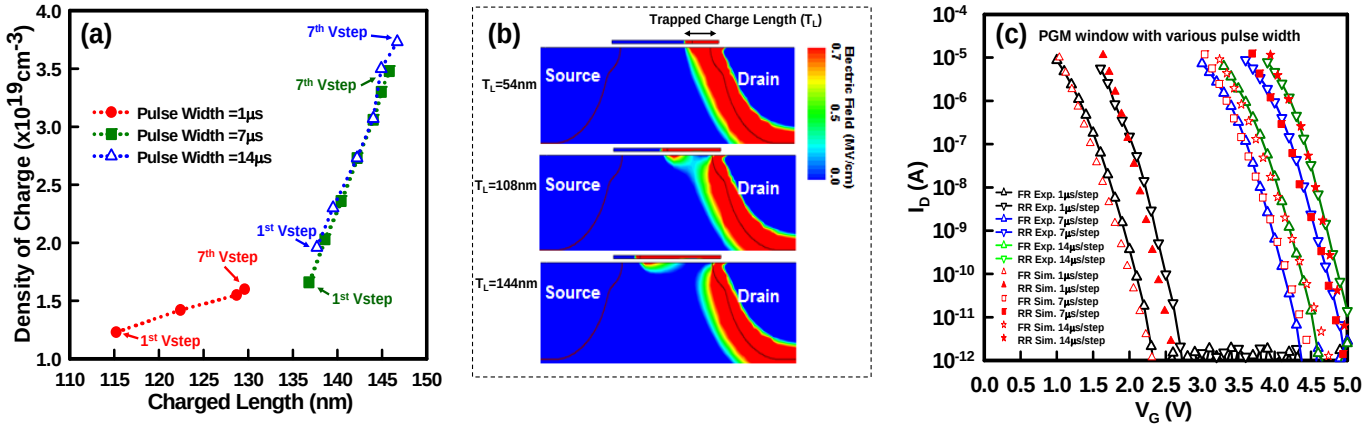

Fig. 5. (a) Simulated trapped charge evolution curve depends on program step number. (b) The Electric field associated with different T_L during PGM period. (c) The measured and simulated PGM window in forward and reverse read with various pulse widths.