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A Process Technology and Characterization for 20nm PRAM

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1. Introduction

Phase-change random access memory (PRAM) has been recognized as a promising candidate to replace conventional memories such as DRAM, NAND FLASH, and NOR Flash because of its scalability, low cost, and high performance [1]. In spite of its prominent properties, PRAM did not show actual significant progress compared to DRAM and Flash devices due to the difficulty of compactly integrating the phase-changed memory (PCM) cell and reducing the programming current without any reliability degradation. In this work, we demonstrated 20nm node size PRAM technology with confined cell structure of PCM and a Si-based PN diode for a memory cell selector. Its cell characteristics and reliability so far obtained were reviewed as well. It implies the strong possibility of PRAM as high density memory for main memory application.

2. 20nm PRAM Technology

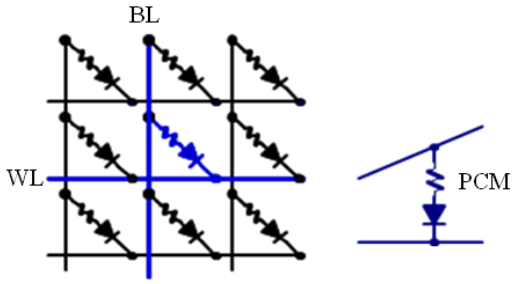
Process Integration

PRAM cell consists of bit-line (BL), PCM, bottom electrode (BE), cell selection device, and word-line (WL) in series. Fig.1 shows the schematic diagram of cell array and unit cell. Confined PCM cell structure and Si-based PN diode using selective epitaxial growth (SEG) technique were used as main integration schemes. The 20nm node size diode contact was fabricated by double patterning technology (DPT). Silicide and W pad were formed on the Si diode. The bottom electrode contact windows were opened on the W pad, followed by forming bottom electrode and confined PCM cell structure. The confined cell structure requires a smaller PCM volume for programming compared to the conventional line-typed cell structure, resulting in smaller programming current (Ireset) by about 50% as shown in Fig.2 [2]. Fig.3 shows a cross-sectional SEM image of fully integrated PRAM device with 20nm node size and a TEM image of the confined cell of 7.5nm width and 17nm length dimension, respectively.

Cell characteristics

Fig.4 shows the resistance-current (R-I) curve of the confined memory cell in 20nm PRAM. The resistance of the PCM starting with initial set-state largely increases at 80μA, and begins to saturate beyond 100~110μA [3]. Set and reset status is clearly separated by the resistance of 2 orders.

The Si diode was designed to provide enough current to program the PCM cell. Fig.5 depicts a typical current-voltage (I-V) curve measured on the 20nm node size Si diode selector. It was found that the diode has a good swing of about 74mv/dec.



(a) (b)

Fig. 1 Schematic diagram of (a) cell array and (b) unit cell

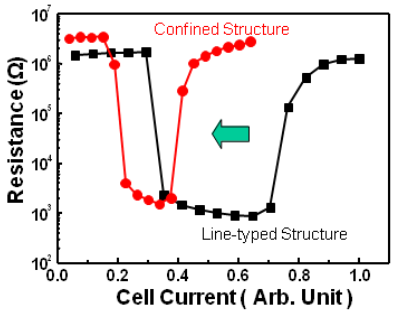
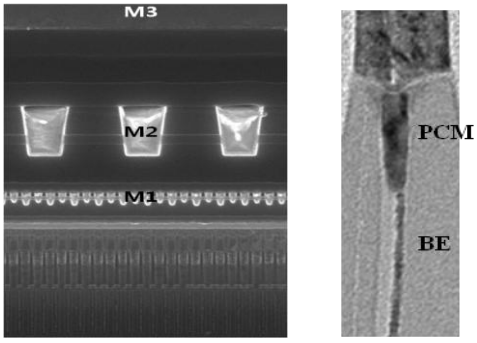


Fig. 2 Cell transition characteristics of confined structure and conventional line-typed structure



(a) (b)

Fig. 3 (a) Cross-sectional SEM micrograph of PRAM cell array and (b) TEM image of confined PCM cell with 7.5nm width

Cell reliability in PRAM becomes one of major concerns as the cell size decreases further and further. It has been reported that the PCM cells fail after the repeated

cycles from PCM delamination or voids due to mechanical stress or phase separation [4]. The cycling endurance can be improved by optimizing a cell structure [5]. We obtained the endurance characteristics over 1E11 cycles with the confined cell structure in this work as shown in Fig.6.

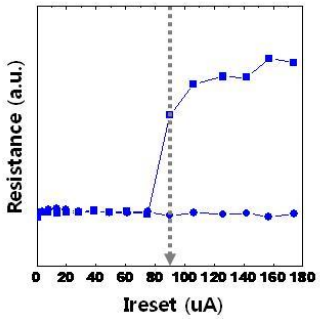


Fig. 4 R-I curve of confined PCM cell with 7.5nm width and 17nm length

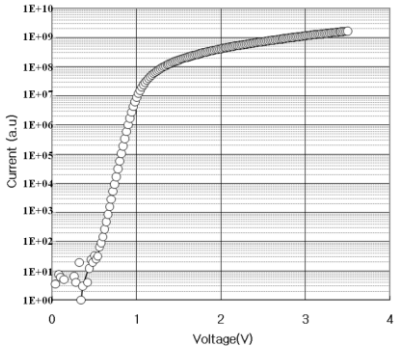


Fig. 5 I-V curve of Si-based PN diode with 20nm node size

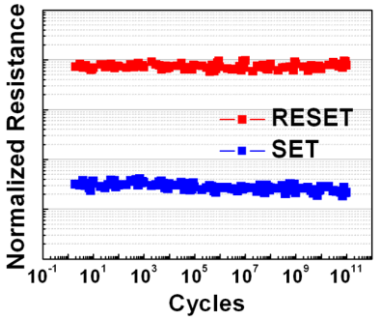


Fig. 6 Cycling endurance characteristics of the confined PCM cell with 7.5nm width and 17nm length

Thermal disturbance is one of critical issues for scaling PRAM. The thermal disturbance strongly depends on the applied programming current and the space dimension between the adjacent cells. In addition to reduce the programming current, the disturbance can be improved by inserting thermal boundary resistance (TBR) between the cells. Comparing the conventional line-typed cells connected with PCM in the BL direction, the confined cells are isolated by dielectrics such as silicon nitride or oxide. Fig.7 illustrates that there is no disturbance failure up to 1M cycles in this work. Fig. 8 shows the extracted data retention time over 10 yrs at 55℃, and activation energy of 2.3eV.

3. Conclusions

20nm node size PRAM has been successfully demonstrated using Si-based PN diode as a selector device and confined PCM cell structure. The programming current was below 100 μA and the diode was optimized to provide enough current to program the PCM. Their set and reset resistance was clearly separated and stable reliability was obtained. It implies that PRAM can be scaled down to 20nm node and below. Further studies are on performing for lower programming current, better reliability, and higher cell density. It is expected that enormous chance to broaden applications of PRAM will come in the near future.

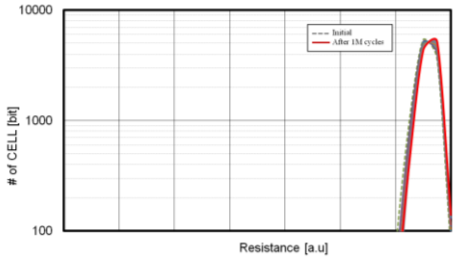


Fig. 7 Reset resistance distribution of the nearest cell according to the number of the programming cycles

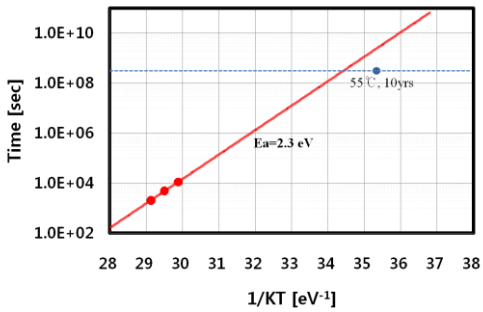


Fig. 8 Arrhenius plot of retention failure time

References

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