Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp618-619

# Formation free and high-performance cross-point resistive switching memory using Ir/$TaO_x$/W structure

A. Prakash[1], S. Maikap[1,*], C. S. Lai[1], W. S. Chen[2], H. Y. Lee[2], F. T. Chen[2], and M. J. Tsai[2]

[1]Department of Electronic Engineering, Chang Gung University, Tao-Yuan, Taiwan
[2]Electronics and Optoelectrolics Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan
[*]Corresponding author: Tel: 886-3-2118800 ext. 5785 Fax: 886-3-2118507 E-mail: sidhu@mail.cgu.edu.tw

## 1. Introduction

Metal-oxide-metal (M-O-M) based resistive random access memory (RRAM) is proving to be front line runner as an alternative choice to replace conventional non-volatile memory devices due to its excellent scalability potential, good CMOS compatibility and simple structure [1-4]. High endurance (>$10^6$), low power consumption and uniformity are extremely important requirements. Moreover, these devices in cross-bar structure are advantageous for 3D stacking. However, materials that require high processing temperature are not preferred for 3D technology. In our previous study, formation polarity dependent resistive switching memory with current compliance of >500 μA was reported [5]. However, the extra step of formation process will increase fabrication cost. In this study, formation free resistive switching properties of Ir/$TaO_x$/W memory device in a cross-point structure fully fabricated at room temperature have been investigated for the first time. Robust pulse endurance of >$10^6$ cycles with only ±2.5 V/100 μA is obtained. The multilevel data storage capability, narrow statistical distribution of memory parameters which are technologically of immense importance, read endurance of >6x$10^5$ times and 85 $^oC$ data retention are also demonstrated. The underlying switching mechanism is successfully explained with supporting electrical data. The surface roughness of bottom electrode and thickness of top electrode played important role to achieve formation free, unifrom and high-performance memory device.

## 2. Experiment

At first, 200 nm thick tungsten (W) film was deposited by RF sputter system on 4" $SiO_2$/Si wafer. Then 4x4 $\mu m^2$ size W bars as bottom electrode (BE) were obtained by photolithography and subsequent etching methods. Another photolithography step was carried out to define the top electrode (TE) bars by lift-off method. A high-κ $Ta_2O_5$ film with a thickness of approximately 15 nm as a switching material was deposited by electron-gun system followed by the deposition of Ir (40 nm) TE by rf sputter system. Finally, lift-off was performed to obtain the final cross-point memory devices.

## 3. Results and Discussion

Fig. 1 shows typical cross-sectional TEM image of fabricated cross point resistive memory device. The thickness of $TaO_x$ and $WO_x$ layers are 15 nm and 10 nm respectively. Fig. 2 shows the EDX spectra of deposited stack layers. The presence of O peak at 0.52 keV in $TaO_x$ and $WO_x$ layers indicate the formation of $TaO_x$ and $WO_x$. Fig. 3 shows the typical SIMS profile of $TaO_x$ film. Strong peak of Ta confirms formation of $TaO_x$. Fig. 4 shows the XPS spectra of $TaO_x$ film. The peaks corresponding to $Ta_2O_5$ 4f doublet with peak binding energies of 26.70 eV ($Ta_2O_5 4f_{7/2}$) and 28.60 eV ($Ta_2O_5 4f_{5/2}$) with peak separation of 1.9 eV are observed. Additionally, peaks corresponding to metallic tantalum ($Ta^0$) with peak binding energies of 21.77 eV ($Ta4f_{7/2}$) and 23.74 eV ($Ta4f_{5/2}$) are also observed. The peaks of $Ta^{+5}$ along with $Ta^0$ oxydation states in the XPS spectra confirm the formation of oxygen difficient tantalum oxide ($TaO_x$) film. Fig. 4 shows 1000 consecutive current-voltage (I-V) hysteresis loops of cross-point memory device where the voltage sweep direction is indicated by the arrows (1 → 4). No forming step was needed to initiate the resistive switching. A small operation voltage of <2 V and current compliance of 100 μA are used. Excellent switching uniformity with small set/reset (1.4/-1.8) voltage and large memory window (HRS/LRS) of >100 is achieved. The set, reset power of the memory device is calculated to be 140 μW and 120 μW respectively, which is low enough for power consuming nonvolatile memory applications. The typical value of average surface roughness of tungsten BE in the cross-points is about 8 nm which is higher than that of the flat surface (~1 nm) memory device (generally formation is needed) [5]. This suggests that the rough surface of BE helps to concentrate the electric field which in turn facilitates and controls the filament formation. This results formation free and uniform resistive switching. To investigate the current conduction mechanism, I-V curve of the positive region is replotted in log-log scale and fitted linearly (Fig. 6). Both LRS and HRS curves fit with trap controlled-space charge limited conduction (TC-SCLC). Oxygen vacancies might serve as trap sites. When positive voltage is applied on TE, oxygen ions migrate toward TE leaving behind $O_2$ vacancies and form an $O_2$ rich layer near TE. The $O_2$ vacancy filament will form which bring the device into LRS (Fig. 7 (a)). On the application of negative voltage, the $O_2$ ions repelled from TE and oxidize the vacancy filament which results HRS (Fig. 7 (b)). Fig. 8 (a) and (b) show device-to-device cumulative probability plot of HRS/LRS ratio and cycle-to-cycle and device-to-device set/reset voltage respectively. The narrow distribution is achieved. Fig. 9 shows the multilevel capability of cross-point memory device by limiting the reset voltage at -2.0, -2.5, -2.7 V which enable the three different data levels corresponding to each reset voltage. This is due to the increase of oxidized filament length with increasing the negative voltage. A comparison of the I-V curves at RT and 85 $^oC$ presented in Fig. 10 shows the semiconducting behavior as the resistance of both the memory states decrease with increase of temperature. This indicates oxygen vacancy filament rather than the Ta metallic filament. Fig 11 shows the excellent read endurance characteristics of >6x$10^5$ cycles. Fig. 12 shows the pulse endurance of >$10^6$ cycles with a small current of 100 μA demonstrating the robustness of the memory device. The device was functional even after 1x$10^6$ cycles. It is observed that the thin (40 nm) TE has shown long ac endurance as compare to the thicker (120 nm) TE (not shown here), which will be favorable for nano-sized device in future. Good data retention characteristics of > 3 hours at 85 $^oC$ are shown in Fig. 13.

## 4. Conclusion

Formation free cross-point resistive switching memory stack of Ir/$TaO_x$/W has shown low set/reset power, high uniformity, long ac endurance of >$10^6$ cycles in 1R configuration with a small current of 100 μA. The rough surface of BE helps to defective $TaO_x$ film and concentrate the electric field which controls easily the formation/rupture of filament. Furthermore, good read endurance of >6x$10^5$ times and data retention of >3 hours at 85 $^oC$ are also achieved. The device will be useful for nanoscale memory applications.

## Acknowledgements

Thanks a lot to National Science Council (NSC), Taiwan, under contract no. NSC-98-2221-E-182-052-MY3 to support this project.

## References

[1] A. Sawa, Mater. Today, vol. 11 (6), pp. 28, 2008. [2] Z. Wei et al., IEDM Tech. Dig., 2008, pp. 293–296. [3] J. J. Yang et al., Appl. Phys. Lett., vol. 92, pp. 232102, 2010. [4] H.Y. Lee et al., Electron Dev. Lett., vol. 31, pp. 44-46, 2010. [5] A. Prakash et al., Jpn. J. Appl. Phy., vol. 51, pp. 04DD06, 2012.

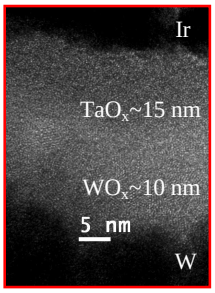


Fig. 1 HRTEM image of the cross point resistive memory device in a Ir/$TaO_x$/W structure. The thickness of high-κ$TaO_x$ film is 15 nm and device size is 4x4 $\mu m^2$.

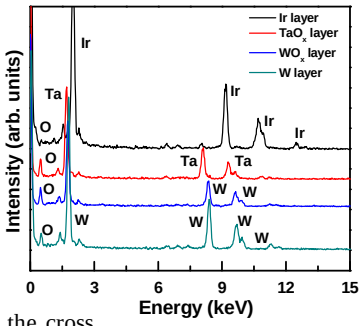


Fig. 2 EDX spectra of memory device. The presence of O peak in $TaO_x$ and $WO_x$ layers indicate formation of respective oxides.

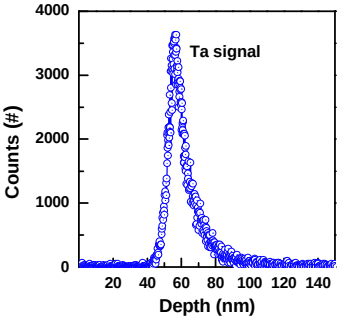


Fig. 3 Typical SIMS profile of $TaO_x$ film.

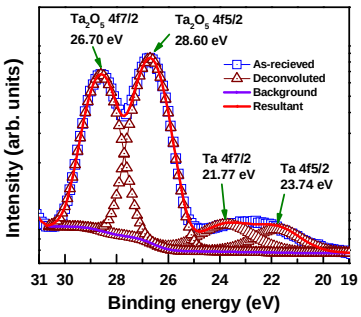


Fig. 4 XPS spectra of (a) $TaO_x$ layer. The peaks of $Ta^{+5}$ along with $Ta^0$ oxydation states in the XPS spectra confirm the formation of oxygen difficient tantalum oxide ($TaO_x$) film

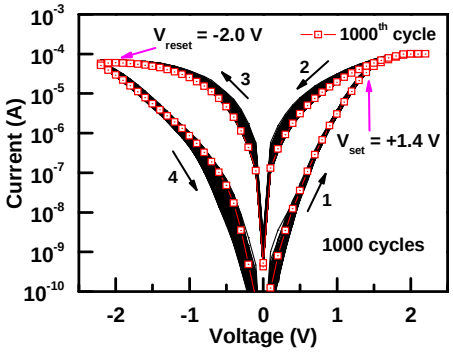


Fig. 5 Current-voltage (I-V) hysteresis characteristics of Ir/$TaO_x$/W cross point memory device. Excellent reversible switching is achieved.

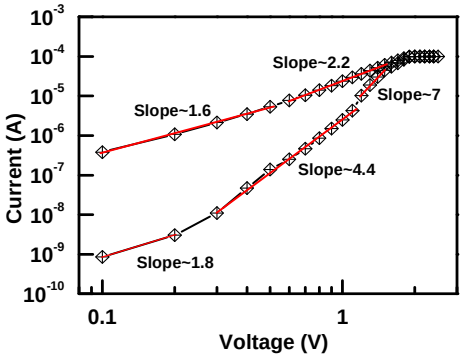


Fig. 6 Log-log plot of I-V curve of positive voltage region fitted linearly. Both LRS and HRS fitted to SCLC mechanism.

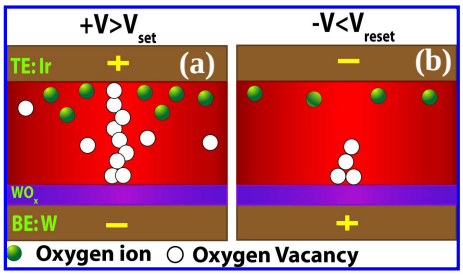


Fig. 7 Schematic representation of proposed switching mechanism based on filamentary model (a) low resistance state (LRS) occurs due to $O_2$ vacancy filament formation (b) high resistance state (HRS) obtained after filament rupture.

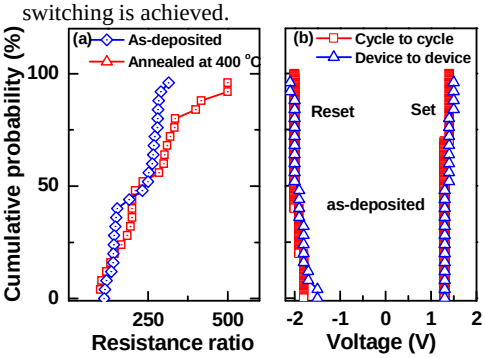


Fig. 8 Cumulative probability plot of (a) HRS/LRS of as-deposited and annealed samples and (b) set/reset voltage. Tight distribution is obtained.

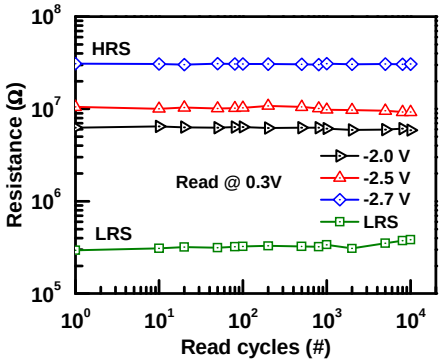


Fig. 9 Multilevel capability of memory device by limiting the reset voltage. Three data levels are obtained at reset voltage of -2.0, -2.5 and -2.7 V.

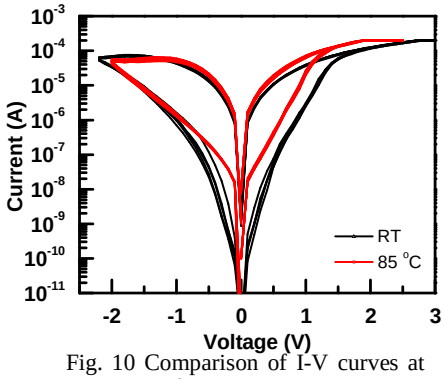


Fig. 10 Comparison of I-V curves at RT and 85 °C. The resistance of both HRS and LRS decrease at 85 °C.

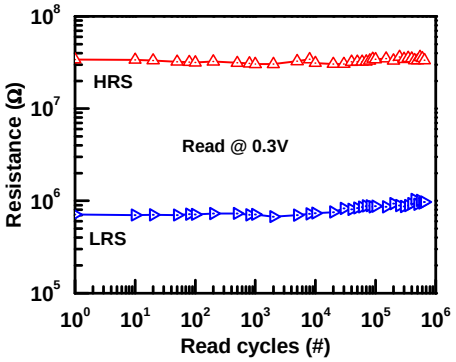


Fig. 11 Good read endurance of >6.5x$10^5$ cycles at read voltage of 0.3V is achieved with no obvious change in HRS and LRS.

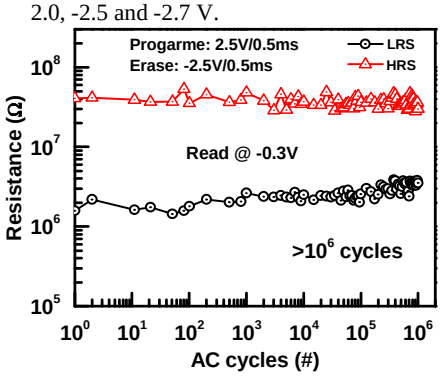


Fig. 12 Excellent pulse endurance of >$10^6$ P/E cycles with small pulse voltage of +/- 2.5 V is obtained. The device was live after $10^6$ cycles indicating much higher endurance capability.

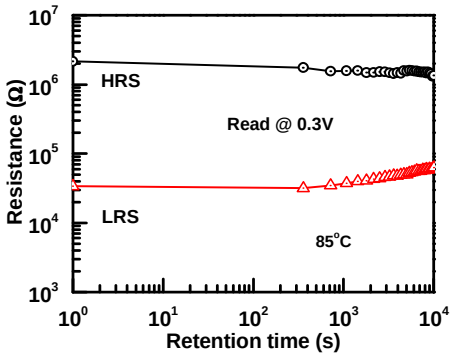


Fig. 13 Retention characteristics of fabricated cross point memory device at 85 °C. Both the memory states were maintained after 3 hours of testing.