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Threshold switching and conductance quantization in Al/HfO_2/Si(p) structures

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1. Introduction

Two main types of resistive switching have been identified in electroformed oxides, namely memory switching (MS) and threshold switching (TS). The difference between MS and TS is that the former is a non-volatile effect while the latter is volatile. MS phenomena are basic for Resistive Random Access Memory (RRAM) operation while TS is important in Phase Change Memories. However, TS effects have also been recently reported in NiO-based MIM structures for RRAM applications [1-4] where TS was attributed to some kind of instability of the conduction filament (CF). In this work, we report experimental evidence of a new kind of TS observed for the first time in Al/HfO_2/Si(p) MOS structures. We claim that this TS phenomenon is not due to CF instability but to the fact that the CF is narrow enough to behave as a quantum wire (QW). No structural modifications of the CF are produced during the SET and RESET transitions, and the whole TS loop can be explained in terms of the electronic properties of the CF itself.

2. Resistive switching and conductance quantization

Al/HfO_2/Si(p) capacitor structures of 120 μm^2 with a HfO_2 layer (~10 nm) grown by Atomic Layer Deposition have been electroformed by successive negative bias voltage ramps with increasing current compliance (Fig. 1) to obtain a stable TS loop under positive gate bias (Fig.2). The TS loop is related to an S-shape negative differential resistance (NDR) which is evidenced when biasing the device with a current ramp (Fig. 3). The TS loop appears as a hysteresis cycle as that of Fig. 2 when using a voltage ramp.

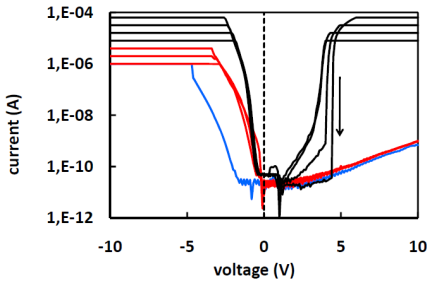

Fig.1 Electroforming by successive voltage ramps from 10V to -10V with current compliance increasing from 1μA to 64μA.

If the CF is wide enough, multiple levels can be observed in the Low-Resistance State (LRS) current branch (Fig. 4), indicating that several 1D subbands play a role and strongly supporting the idea that the CF behaves as a QW. The conduction of the LRS is linear above the holding voltage and the conductance takes values which are integer and non-integer multiples of the quantum of conductance, $G_o=2e^2/h$, as expected for a quantum wire in the high-voltage regime (Fig. 5).

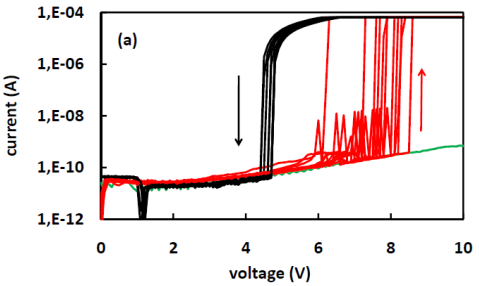

Fig.2 Experimental threshold switching loop. The High-Resistance State (HRS) is controlled by the background injection since the current fully coincides with that before forming (green curve). The SET transitions (red curves) occur in a wide range of voltages while the RESET voltage (black curves) distribution is narrower. In the conduction in the LRS is linear and the conductance is a fraction of the conductance quantum Go=$2e^2/h$.

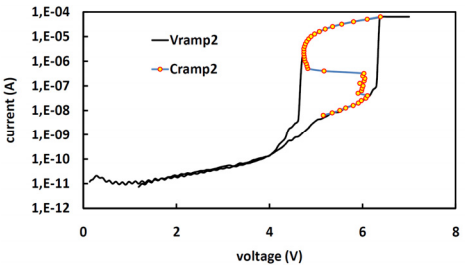

Fig. 3. Threshold switching loop measured with a current ramp (circles and blue line) and a voltage ramp (black line).

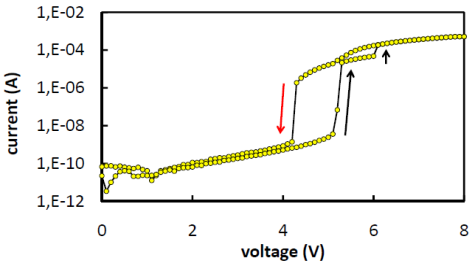

Fig.4 Two-level threshold switching loop. The existence of two sub-branches in the LRS strongly supports the quantum-wire model for the CF conduction. In the present case, the CF was wide enough to present two quantum subbands below the injecting Fermi level in the p-Si substrate

The basics of the QW model [5,6] are presented in Fig. 6 and 7. Fig. 6 highlights the relation between the CF spatial constriction and the quantum confinement potential barrier. The narrower is the CF constriction, the higher is the position of the first quantum subband and consequently, the higher is the potential barrier. Fig.6 shows the band diagrams for the two branches of the TS loop: the HRS (below the barrier tunnel injection) and the LRS (above the barrier transport). Injection from the valence band (VB) of the p-type semiconductor is also a critical factor and it is considered to occur by band-to-band tunneling. This explains the existence of the two different conduction states but, the voltage bistability (S-shaped NDR) requires the existence of two field configurations [7]. These two configurations arise from the energy funneling associated to any interface between 3D and 1D quantum systems. This mismatch introduces a contact voltage drop which strongly depends on the QW current causing the appearance of two voltage spatial profiles: a low bias configuration where most of the applied voltage drops in the substrate depletion layer and a high bias configuration where a significant fraction of the voltage drops at the QW interfaces.

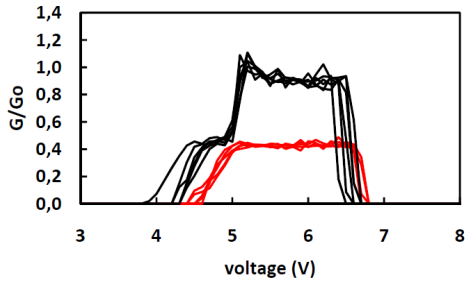

Fig. 5. Normalized conductance during the RESET cycle for a single level CF (red curves) and the two-level CF (black curves). Non-integer multiples of G_o are expected for quantum wires in the high bias regime.

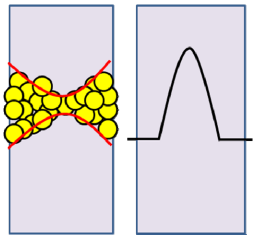

Fig. 6 Left figure: schematic representation of the CF structure (a conducting path made of "defects") with a constriction. Right figure: potential barrier associated to the position of bottom of the first quasi-1D subband in the CF.

Positive feedback changes between these configurations explain the abrupt current transitions observed at SET and RESET. According to this QW model, the barrier height determines the value of V_{RESET} (the holding voltage) and also strongly influences V_{SET}. The barrier thickness modifies the low-voltage transmission and hence it impacts the HRS conduction properties. To the first order, the RESET voltage does not depend on the barrier thickness (bottleneck length) while the SET voltage significantly depends on this parameter because this transition is triggered by noise induced current fluctuations in the HRS [8].

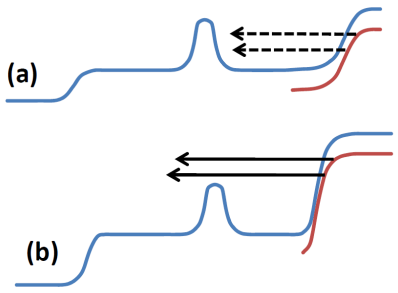

Fig. 7. Schematic energy band diagram to explain the threshold switching model. Injection from the substrate is assumed to take place from the valence band by band-to-band tunneling. Top figure represents the HRS and the bottom figure the LRS. The bistability observed during the TS loop can be explained by the existence of two field configurations.

3. Conclusions

Stable TS loops are obtained by electroforming HfO_2-based metal-insulator-semiconductor structures with a p-type substrate. The reported TS phenomenon is not related to an instability of the CF but to the conduction properties of the nanoscale filament (claimed to behave as a QW) and to current injection from a p-type semiconductor. The strongly non-linear properties of this TS phenomenon might be useful to design RRAM devices without the sneak-path problem. The abrupt current drop at the holding voltage also suggest the possible application to construct TS-based transistors with a steep subthreshold slope.

Acknowledgements

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References

[1] S. Seo et al., Appl. Phys. Lett. **85** (2004) 5655.
[2] J.-W. Park et al., J. Vac. Sci. Technol. B **24** (2006) 2205.
[3] S.H. Chang et al., Phys. Rev. Lett. **102** (2009) 026801.
[4] I. Hwang et al., Appl. Phys. Lett. **97** (2010) 052106.
[5] J. Suñé and E. Miranda, *Tech. Dig. of the International Electron Devices Meeting* (2000) 533.
[6] R. Degraeve et al., *Tech. Dig. of the International Electron Devices Meeting* (2010) 632.
[7] D. Ielmini and Y. Zhang, J. Appl. Phys. **102** (2007) 054517.
[8] S. Lavizzari et al., *Tech. Dig. of the International Electron Devices Meeting* (2008) 215.