Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp642-643

Bipolar Read in ReRAM for 3x Write Speed and 5x Faster Read with Disturb Immunity

Tomoko Ogura Iwasaki[1], Sheyang Ning[2], and Ken Takeuchi[1]
[1]Chuo University, [2]University of Tokyo, 1-13-27 Kasuga, Bunkyo-ku, Tokyo, Japan, E-mail: iwasaki@takeuchi-lab.org

Introduction

ReRAM could potentially bridge the application gap between NAND flash and RAM, due to its high density and high write speeds. Non-volatile buffering capability would significantly improve system performance and simplify reliability in enterprise, as well as, mobile systems [1,2]. For this application, fast read and fast write is required. Set/reset speeds on the order of 20-50ns have been demonstrated, but in order to control resistance variation, read verification between set and reset pulses are needed [3,4]. One drawback of ReRAM is its sensitivity to disturb at low voltages. In order to minimize disturb, the read voltage is generally kept near to 0.1V, which means low cell current and long read times of ~100nsec. This slower read than write is a major obstacle for ReRAM to realize true non-volatile RAM capability. Device/process engineering is on-going to improve read disturb [5,6]. In this work, circuit solutions for reliability and speed are proposed: (i) bipolar verify reduces page write time by 68%, and (ii) reverse read with dynamic write back provides 5x faster, disturb-free read.

Fig. 1 illustrates a bipolar HfO_2 resistor memory element in series with a select gate, characterized by *I-V* curves in Fig. 2 and set/reset operation descriptions in Fig. 3. Fig. 3 also illustrates filament formation according to the filament/oxygen diffusion model [7], in which the filament has been physically observed by oxygen mapping to be wide near the anode electrode and narrow towards the bottom electrode. Set operation uses a positive voltage pulse of 2V to decrease the memory resistance to the Low Resistance State (LRS), and reset occurs by a negative -2V pulse to increase the resistance to the High Resistance State (HRS).

Measurement

Fig. 4a shows memory cell current vs. positive and negative V_{ds} for both LRS and HRS states, and Fig 4b gives the calculated resistance at each read voltage. Resistance decreases exponentially with $|V_{ds}|$, and the slightly higher cell current at +01V vs. -0.1V is attributed to V_{gs} differences in the pass gate. In Figs. 6 and 7, disturb is measured for both forward and reverse read polarities, respectively. Forward read is defined as biasing of the upper anode, V_d, in the same direction as set (corresponds to positive V_{ds} in Fig. 4), and in reverse read, the lower cathode, V_s, is biased in the same direction as reset (corresponds to negative V_{ds} in Fig. 4).

Discussion and Performance Improvement

Regarding forward positive V_d bias and disturb as shown in Fig. 6, once a filament is formed, the LRS filament is stable under the same positive read direction. However when forward read is applied to HRS, instability is observed at 0.5V, which indicates that oxygen trapped in the gap is relatively easy to disassociate. Regarding opposite direction reverse read, shown in Fig. 7, positive bias on the cathode, V_s, stabilizes oxygen and HRS is stable. However, for LRS, disturb is observed at both V_s= 0.3V and 0.5V. This behavior leads to speculation that there could be some field intensification at the sharp filament point, near the small cathode gap, as shown in Fig. 5, which could be similar to the corner field enhancement that has been utilized in floating gate memories [8]. Reverse on LRS disturbs at lower voltages than forward read on HRS.

This work proposes two ways in which reverse read can provide valuable performance advantage without compromising reliability. The ***bipolar verification scheme*** is explained first. In Fig. 8, program and verify operation voltages are described. Bit lines (BL) are connected to the memory drains, and source lines (SL) are connected to the memory sources. Reset verify is performed by reverse read, and set verify utilizes forward read. Since verifies are conducted in the same direction as programming set/reset operations, the voltage can be safely raised to obtain higher cell currents without disturb. In addition, the high capacitance SL does not need to change voltage between verify modes, which reduces the transition time between modes by half. Table 1 compares bipolar verification with conventional verify programming, which uses forward read with V_d=0.1V, for both reset and set verify. According to Fig. 4a's *I-V* curves, by raising V_s to 0.5V in reset verify, sensing cell current increases 8x, from 0.5uA to 2uA. Similarly, in set verify, increasing V_d to 0.3V, raises the current from 2uA to 10uA. Performance improvement is quantified in Fig. 9. Assuming set pulse of 50ns, reset pulse of 20ns, BL capacitance of 2pF, mode transition times of 100ns for conventional and 50ns for bipolar verify, and the set verify and reset verify currents given in Table 1, reset with verify can be reduced by 8x, and set with verify can be decreased by 2x, as given in Fig. 9a. For a single page write operation, shown in Fig. 9b, the total time can be decreased from 2.3usec to 0.8usec, which is a 68% savings.

The second proposal, ***reverse read with write-back*** provides 5x faster read with disturb immunity. The cell voltages for reverse read and write back are described in Fig. 10a, and Fig. 10b shows the basic state diagram. 0.3V reverse read gives 10uA cell current for high speed sensing, so that data can be read out as fast as 20ns, depending on array organization. To handle the eventual LRS disturb, each selected cell is connected to two sensamps, which have separate references, and are operated in parallel. The first sensamp is for normal read, and normal read data is output after 20ns. The second senseamp is used to check the LRS disturb margin, and its reference is increased by some disturb margin, such as 20%. If the margin check result indicates that the LRS resistance increased above 20%, then the cell is written-back with a set pulse. By using reverse read, the voltage of the high capacitance SL can be the same between read and write-back. Also, by using the reverse read direction, the margin check operation can be performed quickly, under the same bias conditions, and in parallel with normal read. (If the read direction is forward, then HRS disturb check would need a separate bias condition from read, which would impact read speed.) Dynamic write back occurs only as needed, so cycling endurance is not unnecessarily penalized. From the V_s=0.3V LRS curve in Fig. 7, 20% resistance disturb occurs after 0.5 hours. Regarding access time is not increased by write-back because read (T_{read}=20nsec) and set (T_{WB}=50nsec) are fast, and transition time between the two operations is minimal. As a further performance enhancement, write-back can be entirely removed from the read time, because it happens so rarely. Whenever write back occurs, the system could be paused with a BUSY signal for a few cycles. Thus, 20ns chip read with no read disturb is possible. This guaranteed read disturb immunity could be very attractive in higher temperature applications where disturb is an especially challenging issue.

Conclusion

By utilizing read in forward and reverse directions, two schemes are proposed to improve chip performance. Bipolar verify reduces page program time by 68%, and fast reverse read with write back improves access time by 5x while guaranteeing disturb immunity.

Acknowledgements

The authors appreciate K.Higuchi, N.Awaya and H. Akinaga for their support. This work is partly supported by NEDO.

References

[1] M. Fukuda, *et al*., Extended Abs. SSDM, p.1166, 2010.
[2] H. Fujii, *et al*., Symposium of VLSI Circuits, 2012.
[3] K. Higuchi, *et al*., IMW 2012.
[4] H. Akinaga, *et al*., Proceedings of the IEEE, Vol. 98, No. 12, p.2237, 2010.
[5] M. Terai, *et al*., Symposium on VLSI Tech, p.50, 2011.
[6] HY. Lee, *et al*., Symposium on VLSI-TSA, p.132, 2010.
[7] Z. Wei, *et al*., IEDM, p.31.4.1, 2011.
[8] Y. Tkachev, IEEE Transactions on Electron Devices, Vol. 59, No.1, p.5, 2012.

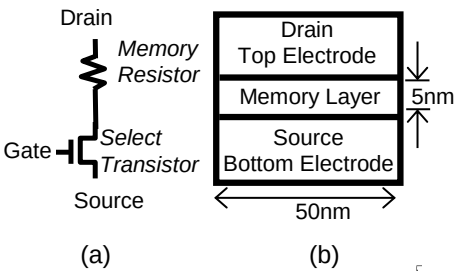

Fig 1: a) 1R+1T memory cell, b) resistor cross-section, memory layer is HfO_2.

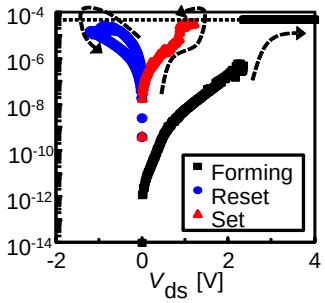

Fig 2: Symmetric bipolar memory cell I-V characteristics [3].

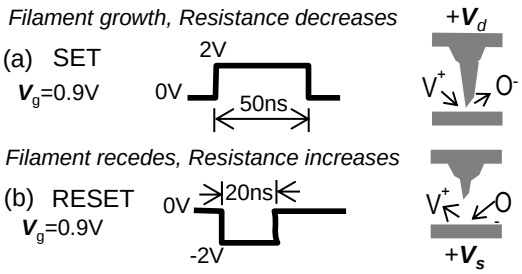

Fig 3: SET and RESET conditions. Filament growth by V^+ vacancy and O^- migration according to oxygen diffusion model [7].

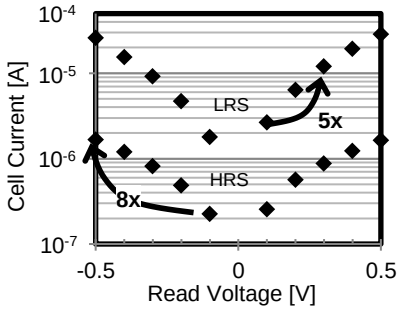

Fig 4a: Measured cell current. Changing HRS read voltage -0.1 to -0.5V increases current by 8x.

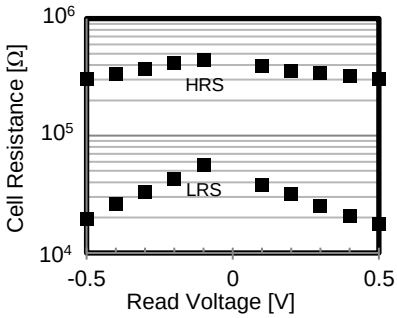

Fig 4b: Cell resistance calculated based on *I-V* in Fig. 4a.

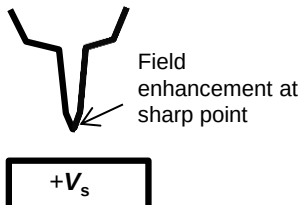

Fig 5: Electric field enhancement at narrow filament point might accelerate reset disturb behavior.

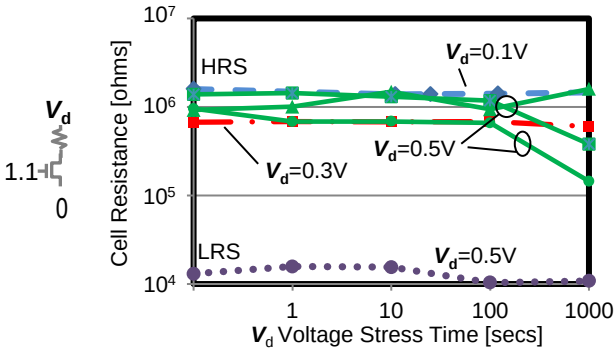

Fig 6: Measured **forward read disturb** @ V_d=0.1, 0.3 and 0.5V. HRS: High Resistance State, LRS: Low Resistance State.

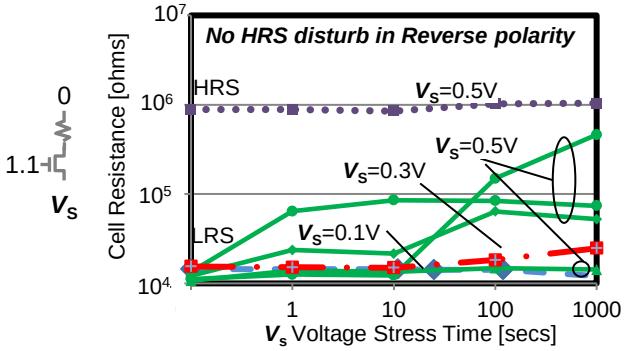

Fig 7: Measured **reverse read disturb** @ V_s=0.1, 0.V and 0.5V. Minimal HRS disturb in Reverse Read at V_s=0.5V.

	Reset (HRS) Verify, R>200kΩ			Set (LRS) Verify, R<50kΩ		
	Direction	Vd [V]	Icell_read [uA]	Direction	Vd [V]	Icell_read [uA]
Conventional	Forward	0.1	0.5	Forward	0.1	2
Bipolar Verify	**Reverse**	**Vs=0.5**	**4**	**Forward**	**0.3**	**10**

Table 1: Summary of bipolar verify proposal vs. conventional. 0.5V reverse voltage on HRS and 0.3V forward read on LRS give higher cell currents.

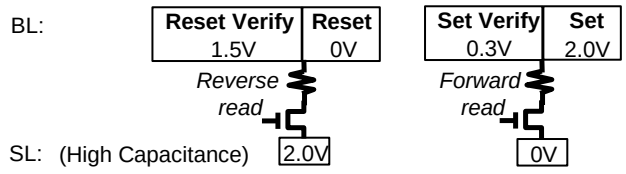

Fig 8: **Bipolar verification scheme**. By reverse read during reset verify and forward read during set verify, the capacitive SL does not need voltage change.. Transition between verify-to-program decreases 50%.

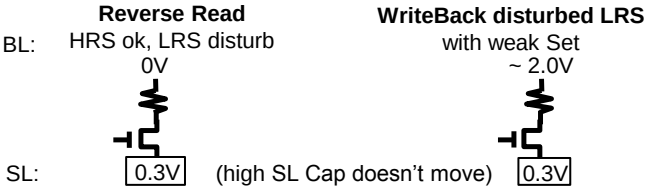

Fig 10a: **Fast read with dynamic write-back concept** for disturb-free, high temp apps. 0.3V reverse read gives 10uA read cell current, write-back only when LRS cell is significantly disturbed.

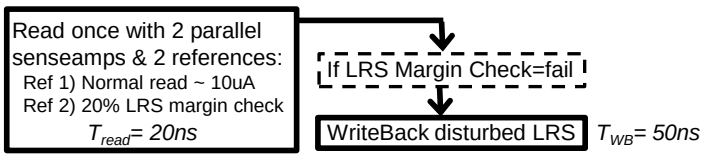

Fig 10b: Read and margin-check are performed in parallel. WriteBack is performed only after 20% margin check fails, (after 0.5 hours according to Fig. 7's V_s=0.3V curve).

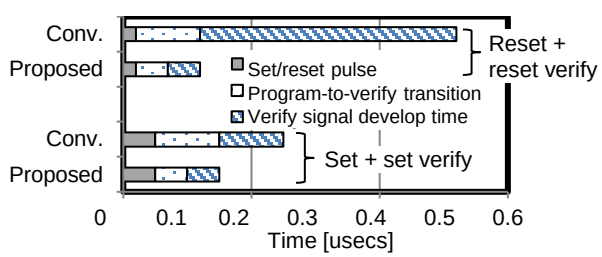

Fig 9a: Conventional vs. bipolar verify, single program pulse. Reset verify decreases 8x, set verify decreases 2x.

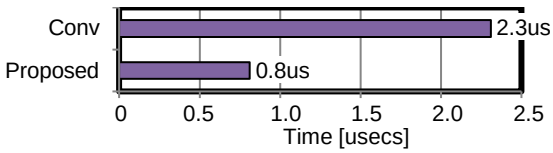

Fig 9b: Single page write time (includes 3 set and 3 reset operations). Bipolar verify reduces page write time 68%.