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Single Contact RRAM in Pure 65nm CMOS Logic Process

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Abstract

In this work, a novel RRAM cell defined by a single contact area is proposed. Cell arrays with the contact RRAM driven by the vertical bipolar transistor underneath have been successfully demonstrated. Bi-directional as well as unipolar set and reset operations can both be achieved. Selecting and driving by a vertical bipolar transistor, this single contact cell (1C-RRAM) can be further scaled to an ultra-small size. In addition, fabricated by 65nm technology, single contact RRAM is fully compatible with advance logic process, hence a very promising solution for future high density and embedded NVM applications.

Keywords:Contact RRAM, Logic NVM, Resistive, CRRAM, Vertical BJT, Embedded Memory

Introduction

Resistive Random Access Memory has become the focus of many memory studies in recent years [1-3], as a result of its strong advantages in scalability, non-volatility, endurance. Its simplicity as well as small size push RRAM device into the development of neuromorphic circuits, which simulates the functions and operations a brain [4]. To model the behavior of a neuron and its thousands of synapses connecting to other neurons, three terminal latching devices have been proposal to realize the memory function in CrossNets[5]. Easy integration of a memory unit and a computation element is the key to simulate the operation of a synapse in neuron communications. The logic compatible contact RRAM cell in our previous studies [6-7] allows the resistive switching element to be implemented side by side to the logic transistors, making it best suited for such applications. In this work, a single contact RRAM (1C -RRAM) cell by adapting a vertical BJT driver underneath the contact RRAM has been demonstrated in 65nm logic node. Without alternations or added processing steps, this "One Contact" memory can allow the further scaling of this new logic NVM for future large scale, neuron logic circuit applications.

Fabrication and Architecture

The cross-sectional illustration of the proposed 1C-RRAM cell is shown in Figure 1(a). The RRAM film consists of SiO2, TiON and TiN stacked layers, as revealed by the TEM picture in Figure 1(b), are placed underneath the W contact, while aligns on top of a vertical npn bipolar transistor. This vertical npn transistor fabricated by standard logic process is formed by n-LDD emitter, p-pock base and n-well collector, as discuss in our previous work [8]. The simulated doping profile of this vertical BJT is shown in Figure 1(c). The contact RRAM landed directly on the n-LDD emitter regions to form a vertical cell structure. A simple NOR-type array with buried diffusion WL connected the BJT base regions and metal-1 layer with contacts to the RRAM top layer are illustrated in Figure 2(b) and demonstrated by the cell array in Figure 2(b). As shown in Figure 2(b), a single RRAM cell can be defined by only one contact area, reaching the 2D limit of $4F^2$ when design rules allow.

Results and Discussion

To investigate the basic operation characteristics of this 1C-RRAM cell, the set and reset characteristics are reviewed in Figure 3, revealing that this RRAM operates under 4V with WL control at 0.9V and 1.3V, respectively. The read current ratio highly depends on the read bias condition on both the WLs and SLs. As summarized in Figure 4, the highest current ratio between the two states can obtain under a high WL voltage of 1.5V, while SL is biased at 1V. The basic operation conditions of this 1C-RRAM array are summarized in Table 1, where both the forward and reserve conditions are used for set and reset operations, indicating the non-polar characteristics of the contact RRAM film. The DC cycling results in Figure 5 present an on/off window of 8X between the high and low resistance states. The time to set characteristics shown in Figure 6 indicates a set time of less than 100μsec can be achieved with V_{BL}=4V. This cell however required a much longer reset time, close to 0.5msec. As suggested by our previous study [9], the random telegraphic noise (RTN) in contact RRAM cell affects the read current variability. As shown in Figure 7, the read current characteristics can be greatly affected by the RTN signal, suggesting that the trapping and de-trapping of electrons in the RRAM film may induce a read error in large arrays. Another interesting characteristic of this 1C-RRAM cell is that the cell can be read in both directions. As compared in Figure 8, the read current characteristic of the two states under forward and reversed can be distinctively different as a result of the asymmetric performance of the vertical BJT driver. Figure 9 monitors the read current levels under continuous read stress. This read disturb test reveals stable read current levels for more than 1000 seconds. Finally, the data retention results under 150°C baking test are shown in Figure 10. As expected, the single contact RRAM exhibits excellent data retention capability, same as that observed in contact RRAM (CRRAM) devices.

Conclusions

In this work, the first demonstration of "one contact" RRAM cell in 65nm standard logic technology is presented. Its basic operation conditions and functions have been successfully demonstrated by a test array with buried wordline controlling the base of the vertical BJT driver. Its non-volatility, high density, and full logic compatibility can bring the realization of and large-scale neuromorphic nano-electronic circuit one step closer to reality.

References

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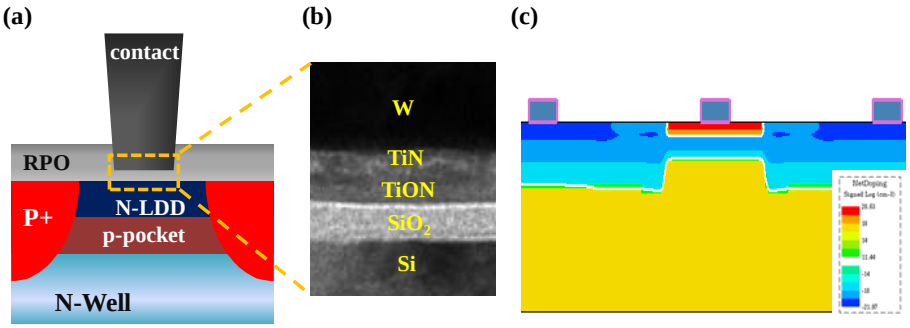

Figure 1 (a) Cross-sectional view of the single contact RRAM (1C-RRAM) cell fabricated by pure 65nm CMOS logic process and (b) HR-TEM pictures of the switching resistance film (c) Doping profiles of the vertical npn BJT.

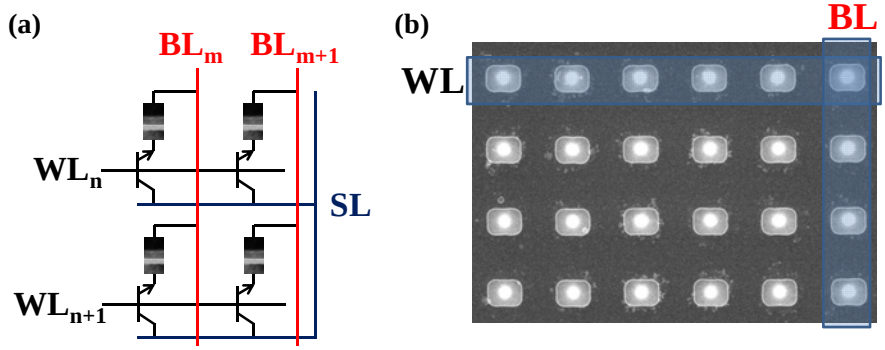

Figure 2 (a) The 1C-RRAM cells arranged in a NOR type array (b) Top view picture of 1C-RRAM array, where the WL are connected by the buried p+ diffusion, while the BL by metal-1 to the top contacts.

	Reverse Direction				Forward Direction			
	Forming/Set		Reset		Read		Reset	
	Sel.	Unsel.	Sel.	Unsel.	Sel.	Unsel.	Sel.	Unsel.
WL	0.9 V	Float	1.3 V	Float	1.2 V	Float	3 V	Float
BL	4 V	Float	2.8 V	Float	0 V	Float	0 V	Float
SL	0 V	0 V	0 V	0 V	1 V	1 V	2.2 V	2.2 V
P-SUB	0 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V

Table 1 Operation conditions of 1C-RRAM cells arranged in a NOR type array under both forward and reverse directions.

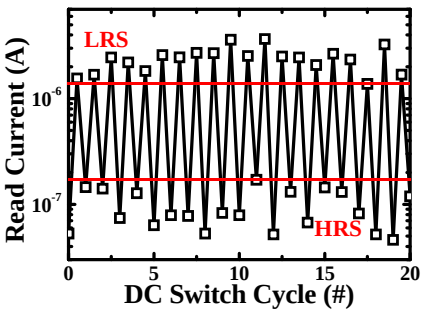

Figure 5 Resistance switching cycles in DC measurement and two read current levels are divided by an 8X sensing margin.

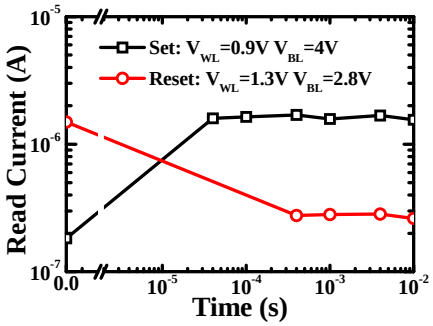

Figure 6 Time to set/reset characteristics reveals a longer reset time is required.

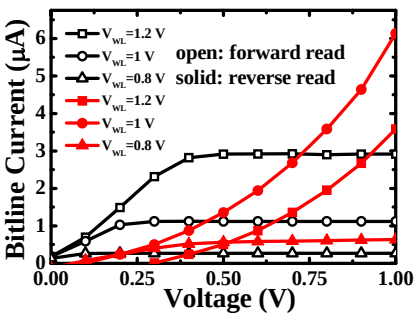

Figure 8 Distinctive read characteristics in both directions can be used for further optimizations of the operation conditions.

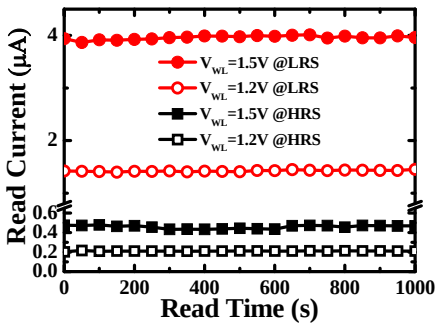

Figure 9 Read disturb characterization under different WL voltages shows very little change in its read current levels.

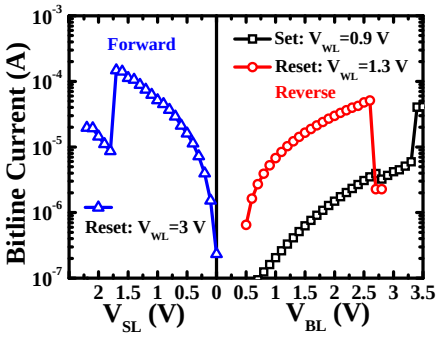

Figure 3 DC characterization of 1C-RRAM for set and reset operations both in reverse direction, or the reset operation is opposite to forward direction.

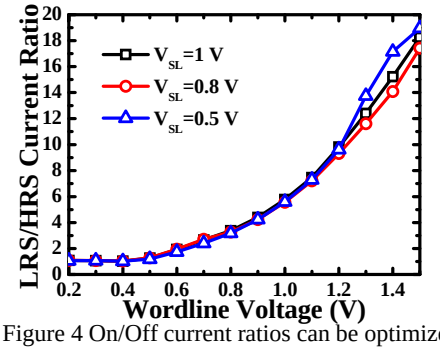

Figure 4 On/Off current ratios can be optimized by read condition adjustments.

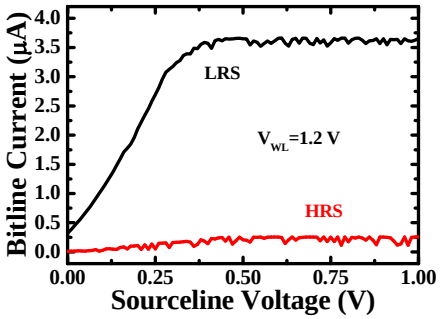

Figure 7 Read variability of 1C-RRAM can be problematic in large cell arrays.

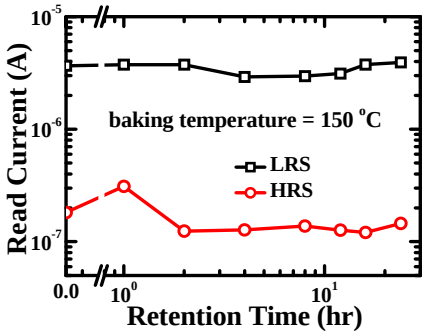

Figure 10 Stable levels can be maintained in the 1C-RRAM even under high temperature bake.