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# Characterization of carbon nanotube based vertical interconnects

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## 1. Introduction

Carbon nanotubes (CNTs) are widely studied as an alternative for Cu interconnects because of their exceptional, electrical and thermal properties [1]. Employing these properties in practical application requires a lot of technological challenges to be solved. In this paper we study electrical properties of CNTs integrated as a vertical interconnect for CMOS technology. CNTs were integrated in ϕ =150nm contacts using the toolset of 0.13µm node Cu platform at imec in combination with a dedicated plasma CVD tool (Tokyo Electron Ltd) for low temperature CNT growth. The work reports on the characterization of different aspects of the vertical interconnect, in particular CNT to metal contact and CNT shell quality for growth temperatures between 400 and 540°C.

## 2. Process for CNT integration in 150nm contacts

The CNT contacts were fabricated on 200mm Si wafers with TiN as conducting bottom layer [2]. On TiN, 50nm $Si_3N_4$ was deposited followed by 360nm PSG oxide and 30nm SiC. The 150nm holes were etched and the process was finished with a 60s of 0.5% HF wet etch to create an undercut. The Ni catalyst was deposited using PVD and preceded by an Ar sputter clean. A Ni layer with on-field thickness of 3nm was deposited in order to reach ~1 nm at the bottom. Sidewall deposition was minimized by the HF undercut while the top SiC ensured selective CNT growth[3]. Growth was done in a remote plasma CVD reactor at wafer temperatures ranging from 400°C to 540°C. After break-up of the Ni, CNTs are grown using a $C_2H_4/H_2/Ar$ mixture. CNTs were encapsulated in 15nm ALD $Al_2O_3$ plus 60nm sub-atmospheric chemical vapor deposition (SACVD) SiO2 layers [2] to provide mechanical strength to CNTs for the subsequent chemical-mechanical polishing. This CMP was used to remove excessive material and planarize the stack. The process continued with the deposition of the Metal1 dielectric stack followed by a Metal1 trench etch. During this etch the CNT tips are exposed to the dielectric etch plasma and the strip. A dedicated clean step just before metallization was implemented on some wafers to study the impact of the tip clean. All wafers continued for 15/10nm TaN/Ta barrier deposition followed by Cu metallization and a SiC passivation layer. Fig. 1 shows the cross sectional view of the CNT contacts.

## 3. Electrical and Morphological characterization of the CNT interconnect

The resistance, $R_{single}$, for a single contact filled with CNTs can be split into 3 main contributors (Fig. 1) consisting of the top interface resistance ($R_1$) at the CNT to top metal (TaN) interface, the resistance ($R_2$) resulting from the length of CNT itself, and a resistance ($R_3$) from the bottom interface at the TiN to CNT interface. Ideally, the bottom plus top contact interface resistance consists of the quantum resistance of 6.5kΩ per shell [1] with no contribution from the ideal metallic CNT that can reach ballistic transport ($R_2$ =0) over sub µm length.

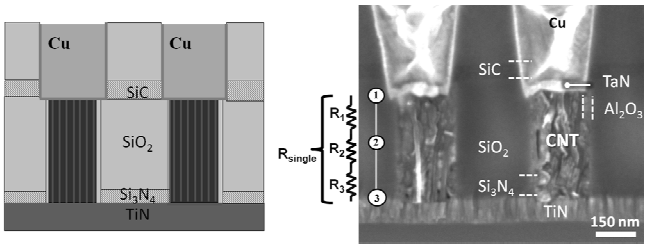


Fig. 1: Schematic and SEM cross section view of CNTs integrated in 150nm contact holes

The top resistance ($R_1$) was studied by implementing a 60s APM clean after damascene etch. The purpose of this clean is to selectively remove the ALD $Al_2O_3$ encapsulation around the tips of the CNT and increase the contact area for the CNT to TaN interface. A reduction of $R_{single}$ was measured compared to samples without this clean step. The resistance was measured on single 150nm contact hole using 4 point probing at 96 locations on the wafers. The box plot (Fig 2.) shows a more uniform distribution for the cleaned contacts and a reduction of the median value from 4.8kΩ to 2.8kΩ.

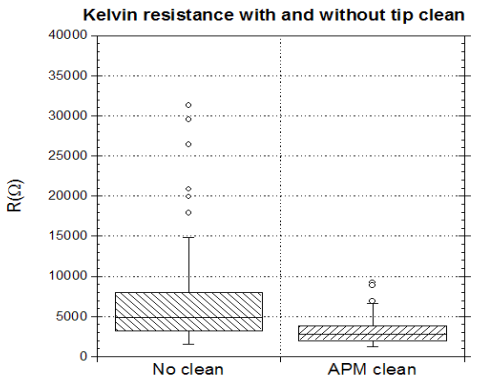


Fig. 2: Full wafer electrical measurements for CNT contacts with and without APM tip clean

In order to evaluate the CNT resistance $R_2$, CNTs grown at temperatures between 400°C and 540°C were compared electrically and morphologically.

Fig. 3 shows both the structural quality of the shell structure and the corresponding electrical measurements. A degradation of graphitization of the shells by lowering the temperature is visible as a morphological change from aligned parallel shells for the 540°C process to bamboo-like structures at 400°C. Electrical comparison of the samples resulted in a surprising decrease of $R_{single}$ for a decreasing temperature.

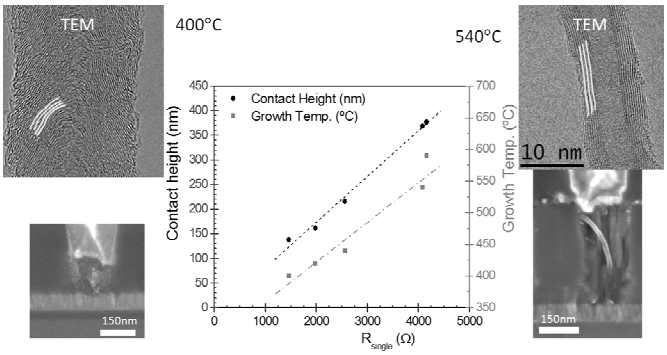


Fig 3: $R_{single}$ as function of growth temperature and length. TEM and SEM images show the structural differences between processes at 400°C and 540°C

Length analysis showed that, after full processing, the contact height was significantly lower for the low temperature wafer. This can be explained by a difference in CMP behavior due to variations in initial length of the CNTs, amount of amorphous material in the field areas, and densification of the $SiO_2$ in between the holes. Comparing the two curves in Fig. 3, we see that the resistance change is more likely to be related to a length scaling than change in CNT quality. In other words, clear differences in CNT quality are not reflected in change in $R_{single}$. The scaling of $R_{single}$ with the length also implies that the electrical behavior is far from ballistic.

Studying the CNT bottom resistance ($R_3$) proves difficult. Any change to the bottom interface layer or catalyst deposition inevitably has an effect on the CNT growth, density, and quality. Differentiating between contributions of the bottom contact changes from the other parameters in growth properties proves very challenging. From TEM pictures on the bottom contact, we found individual shells and CNT caps in direct contact with TiN, indicating both tip and base growth.

Fig. 4 shows the calculated contact resistivity for data found in literature. To benchmark with other groups, we normalize the results to compensate for the variety of sizes and aspect ratios used. Most results are in the same range despite the variety of processes, dimensions, and growth temperatures. The temperature is known to have an impact on CNT structural quality. However, no correlation between growth temperature and the electrical resistivity is seen.

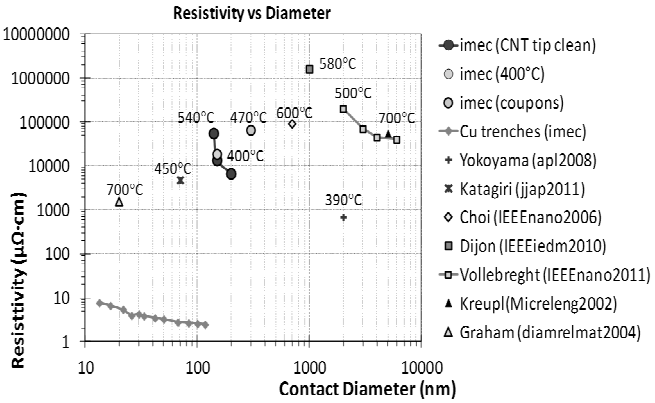


Fig. 4: Comparison of experimental data for CNT resistivity.

## 5. Conclusions

We report on an ongoing study to characterize the electrical properties of CNTs used as vertical interconnects. Improvement in top contact was achieved by applying a tip clean before metallization. A morphological degradation of the CNT quality was observed when decreasing the temperature from 540 to 400°C. This change in quality was not reflected as change in $R_{single}$ indicating that the resistance is not dominated by the CNT only but other process parameters or contact resistances still dominate the performance.


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