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Fully Encapsulated Gate-All-Around InAs Nanowire FET

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1. Introduction

Semiconductor nanowires (NWs) are attracting growing interest as promising building blocks for next generation nanoelectronics devices. InAs NWs are of particular importance in view of application to high-speed, low-power-consumption field-effect transistors (FETs) due to the intrinsic high electron mobility in InAs exceeding that in widely used Si. However, in NW devices the electron mobility is drastically degraded by surface scattering due to the large surface-to-volume ratio combined with the tendency of electrons to accumulate near the surface.

We fabricate an InAs NW FET with a gate-all-around (GAA) structure that enables improved electrostatic control of the channel conductance. In order to realize GAA structure, we adopt a novel two-step gate electrode formation method, where a NW is sandwiched between the lower and upper gate metals. This method allows us to make the gate electrode overlap the source/drain electrodes, leading to a dramatic increase of driving current compared with the previously reported NW FETs without the gate overlap [1, 2]. This may be attributed to the enhanced electron mobility due to surface passivation by the gate metal, as well as to an elimination of the parasitic resistance arising from the gap region between the gate and source/drain electrodes.

2. Experimental method and results

InAs NWs are grown via the Au-catalyzed vapor-liquid-solid (VLS) mode in a MOVPE system [3]. The as-grown NWs are conformally coated with 6 nm of Al_2O_3 via atomic layer deposition (ALD). Then, the NWs are sonicated in isopropanol and dispersed on a Si substrate covered with 500 nm of SiO_2. This device substrate is prepatterned with a Ti/Au lower gate electrode as schematically shown in Fig. 1(a). Here, the upper half of the gate electrode is narrower than the lower half, and their edges including the sidewalls are covered with 40 nm of SiO_2. Next, source and drain Ohmic contact regions are defined by electron-beam lithography (EBL) at both ends of the NW, such that the source/drain electrodes are separated from the exposed gate metal to avoid short circuit, but overlap the gate electrode region buried beneath SiO_2, as schematically shown in Fig. 1(b) and 1(c). In order to ensure good Ohmic contacts, Ar plasma etching is employed to remove the surface oxides at the contact regions of the NW, followed by *in situ* deposition of Al, used as Ohmic contact metal, without breaking vacuum. The Al surface is oxidized in an O_2 plasma to form an Al_2O_3 insulator in order to ensure electrical isolation between the upper gate metal and the Al source/drain electrodes. The upper gate region is defined by EBL so that it overlaps the source/drain electrodes, and angled depositions of Ti/Au are carried out twice from different sides of the NW. Figure 1(d) shows a schematic cross-section at the NW center indicating a GAA structure realized this way. Figure 1(e) shows a scanning electron micrograph (SEM) image of the fabricated GAA NW FET device, whose gate length L_g (equal to source-drain separation) and channel diameter d are 200 nm and 100 nm, respectively.

DC electrical characterizations are performed using a semiconductor parameter analyzer (Agilent B1500A) at room temperature. Figures 2(a) and 2(b) show output and transfer characteristics, respectively, of the device shown in Fig. 1(e). These data show n-type depletion mode FET operation with the threshold voltage of -0.8 V. Maximum drain current I_d = 208 μA is obtained at gate voltage V_g = 2.5 V and drain voltage V_d = 0.5 V. This maximum driving current corresponds to 660 μA/μm when normalized by the wire circumference, $w = \pi d$. Similarly, normalized peak transconductance of 400 μS/μm is obtained at V_g = 0.2 V for V_d = 0.5 V. These values compare favorably with the best values reported in NW FETs [4, 5], which may be attributed to the enhanced electron mobility due to screening of residual ionized impurities by the surrounding gate metal, as well as to an elimination of the parasitic resistance.

3. Conclusions

We have fabricated an InAs GAA NW FET whose gate overlaps source and drain electrodes. It features normalized maximum driving current of 660 μA/μm and transconductance of 400 μS/μm, respectively, at room temperature, comparable to the best NW FETs.

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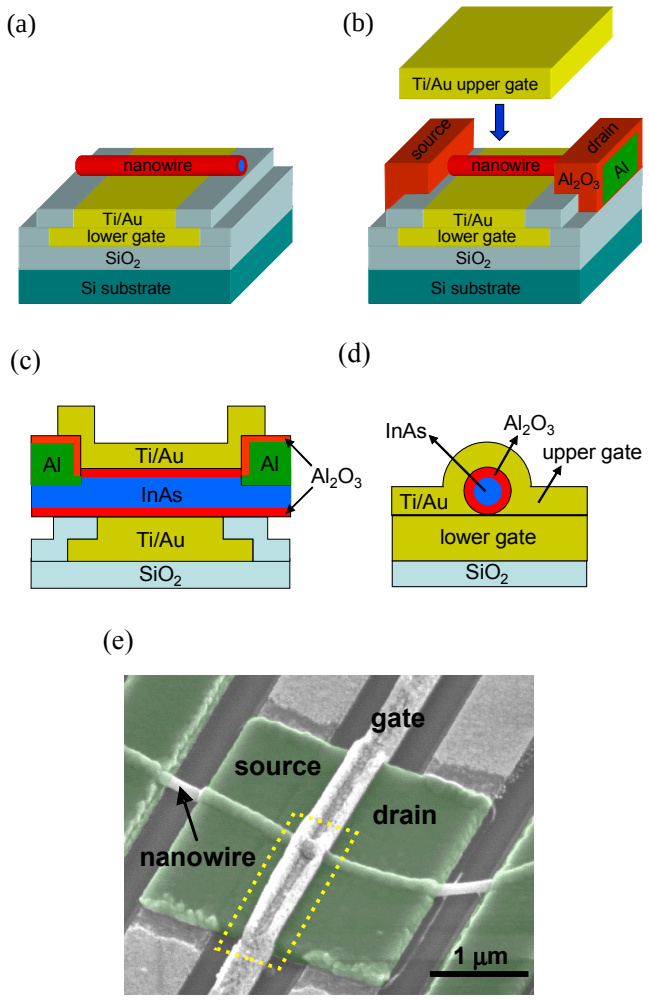

Fig. 1 (a) Schematic device structure before deposition of source/drain electrodes and an upper gate electrode. (b) Schematic device structure of the GAA NW FET with an overlapping gate. (c) Schematic cross-section along the NW axis. (d) Schematic cross-section perpendicular to the NW axis at the center of the FET. (e) False color SEM image of the fabricated device. Green regions denote Al Ohmic contacts with oxidized surfaces. The region enclosed by a dotted line denotes central part of the device schematically shown in (a) and (b).

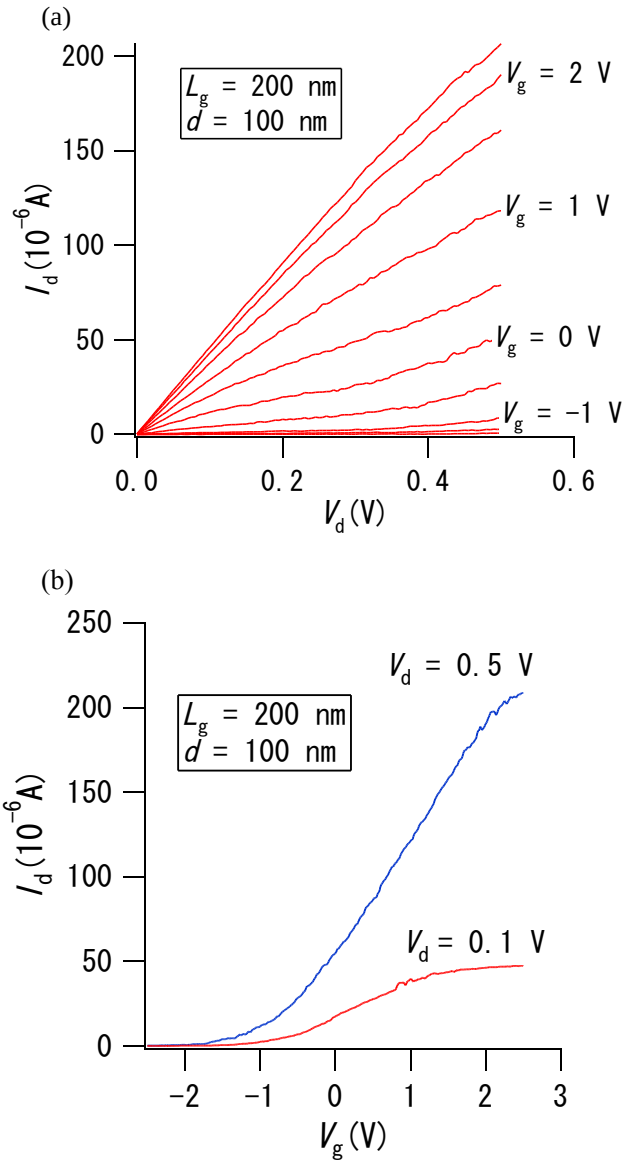

Fig. 2 (a) I_d - V_d characteristics for V_g between 2.5 V and -2.0 V in 0.5 V steps. (b) I_d – V_g characteristics for V_d = 0.1 V and 0.5 V.