

Progress and Challenges in Large-scale Graphene Technology for RF Applications

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1. Introduction

Impressively high current density and carrier mobility exhibited by graphene make it a potential candidate for the future channel material in RF devices [1, 2]. Several graphene RF reports have moved beyond device-level demonstration (i.e. f_T , f_{max}) and showed functional graphene circuits [3, 4]. Recently, full wafer-scale graphene devices processed entirely in a standard 200 mm silicon fab were also demonstrated [5]. In this paper, we will review the progress and the challenges of employing this material in RF applications.

2. Graphene Transistors and Circuits

Although high quality graphene flakes can be easily obtained by exfoliation of graphite, this is not a process that can be used in large scale fabrication. Two main methods have been developed to synthesize large scale graphene films: epitaxial graphene growth on SiC substrates [6] and CVD growth of graphene on Cu [7]. We use both materials for high-speed transistor fabrication. The size of CVD graphene is not limited by expensive starting materials and can be easily expended to 12-inch or above. CVD graphene can also be transferred onto virtually any substrates, which enables new application domains such as transparent or flexible electronics. One of the most challenging issues in graphene device fabrication is to establish a high-quality ALD or CVD gate dielectric on graphene's inert surface (Fig. 1). Several seed layers were developed to provide the nucleation sites for ALD process, including oxidized PVD Al, and spin-coated polymer (NFC). Despite the demonstration of high device f_T (the mobility is preserved), the scalability and manufacturability of these seed-layer enabled gate dielectrics are questionable.

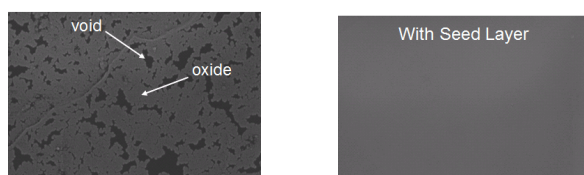


Fig. 1 (Left) SEM image of ALD gate dielectric on graphene without seed layer. (Right) Gate dielectric with NFC seed layer.

Another approach is to transfer CVD-grown graphene onto wafers with pre-defined embedded gate structures—completely eliminating the need of depositing a dielectric on graphene (Fig. 2). To reduce the gate resistivity (to improve device RF performance), an inverted-T gate structure can also be employed to maximize the cross-sectional area of the gate, which is shown in Fig. 3 [5]. Compared to the top-gate structure, the embedded gate design largely simplifies the process of making T-shaped gates and avoids the parasitic capacitance between gate and S/D electrodes.

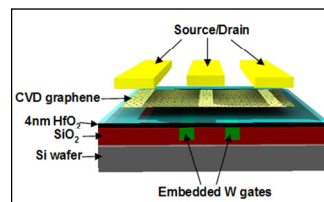


Fig. 2 Schematic of the embedded gate structure. CVD graphene pieces were transferred onto an 8-inch wafer with pre-patterned metal gates covered by a high quality high-k dielectric.

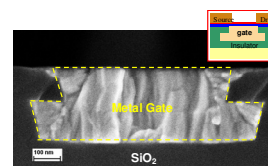


Fig. 3 Cross-sectional SEM image of post-CMP wafer showing the inverted-T gate structure.

One major challenge for the graphene device operation is to obtain drain current saturation, which arises from its gapless band structure. A weak saturation-like output characteristic (or “kink”) has been observed frequently in graphene transistors. This is mainly due to the ambipolar nature of graphene. At certain drain bias, the charge neutrality point moves into the channel, and the drain current shows a saturation-like behavior. Further increase of the drain bias makes the conduction type near the drain-end change from n-type (p-type) to p-type (n-type), and the drain current shows a second linear region. A recent theoretical study suggests that thinning the gate dielectric can lead to strong current saturation in graphene FETs by at least three mechanisms: it reduces the impact from thermally excited carriers, it accelerates the carrier depletion in graphene due to the strong quantum capacitance limit, and it significantly reduces the influence from interface traps [8]. The abovementioned embedded gate provides the thinnest possible gate dielectric. Output characteristics from a PFET and an NFET with 500 nm channel lengths at various V_{gs} are shown in Fig. 4 (a) and Fig. 4 (b), respectively. The drain current saturation can be

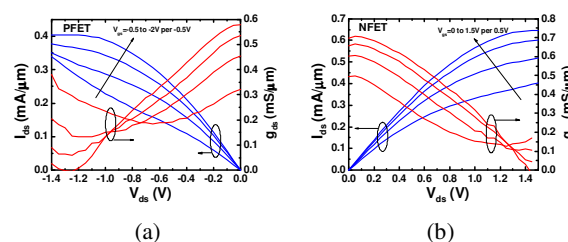


Fig. 4 (a) Output I_{ds} - V_{ds} for PFET operation at different V_{gs} . (b) I_{ds} - V_{ds} for NFET operation. Both PFET and NFET show clear drain current saturation

clearly seen at relatively low V_{ds} from both polarity devices.

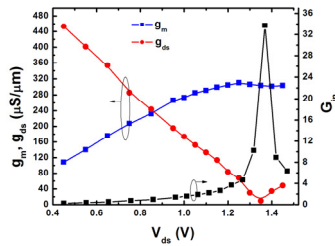


Fig. 5 Measured g_m , g_{ds} , and $G_{in}=g_m/g_{ds}$ across a range of drain bias at $V_{gs}=1.2$ V.

A crucial figure-of-merit for analog/RF transistors is the intrinsic voltage gain (g_m/g_{ds}) which requires both high g_m (primary component of f_T) and low g_{ds} . Due to this saturation and very high g_m from a thin gate dielectric, these devices feature high DC voltage gain (as high as 34, Fig. 5) that is comparable to semiconductor FETs with bandgaps.

Several graphene circuit demonstrations have also been reported recently. Fig. 6 shows the first high-frequency graphene voltage amplifier. The amplifier shows ~5dB low frequency gain with the 3dB bandwidth greater than 6 GHz. The amplifier shown here, consisting of a graphene FET and a high load impedance, was also simulated in a RF circuit simulator, showing that the device is capable of voltage amplification for frequencies exceeding 15 GHz [3].

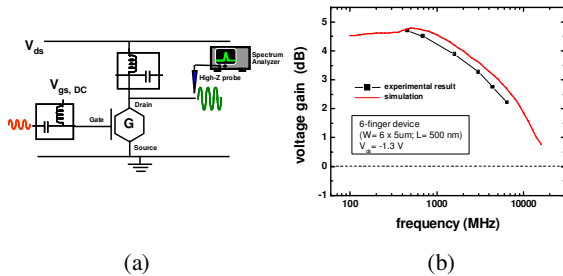


Fig. 6 (a) Schematic of the graphene amplifier measurement technique. (b) Measured and simulated frequency response of the amplifier's voltage gain.

We also demonstrated both GHz-range CVD graphene and SiC graphene circuits where all circuit components, including graphene FET and inductors, were monolithically integrated on a single wafer. Fig. 7 (a) shows the image of fabricated SiC graphene IC on a 2-inch SiC substrate. The integrated circuit operates as a broadband RF mixer with frequencies up to 10 GHz. Fig. 7 (a) also shows a snapshot of output spectrum of the mixer taken directly from the spectrum analyzer with RF input signal $f_{RF} = 3.8$ GHz and LO signal $f_{LO} = 4$ GHz. The frequency mixing is clearly visible with two peaks observed at frequencies $f_{IF} = f_{RF} - f_{LO} = 200$ MHz and $f_{RF} + f_{LO} = 7.8$ GHz [4]. Similar integration was performed with CVD graphene, where a 4-turn inductor (targeting $L=5$ nH) was monolithically integrated with a 6-finger graphene FET (Fig. 7 (b)). The fabricated IC was measured as a frequency doubler. The measured output

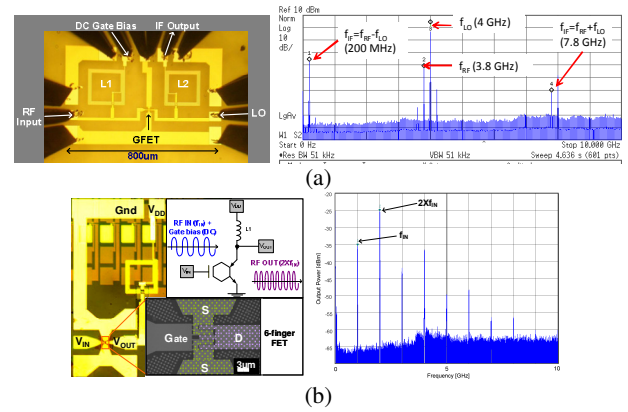


Fig. 7 (a) Photograph of graphene IC using SiC graphene and measured mixer output spectrum. (b) Image of CVD graphene frequency doubler IC and captured image from the spectrum analyzer during the circuit operation.

power spectrum for an input frequency (f_{IN}) of 1 GHz is shown in Fig. 7(b). This doubler features a conversion gain of ~25 dB for an output frequency of 2 GHz with a rejection of the fundamental tone and other frequency components of more than 10 dB. One unique feature of these graphene ICs is their outstanding thermal stability with little performance variation up to 200 °C, significantly better than circuits using conventional semiconductors [5].

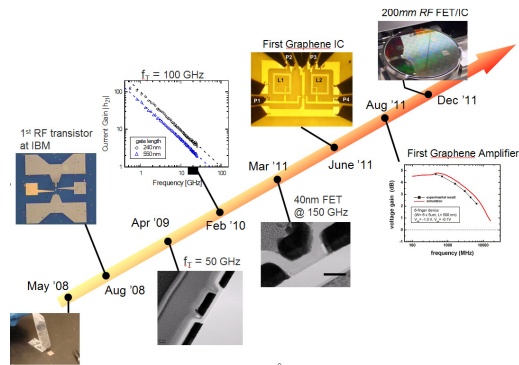


Fig. 8 Important milestones of IBM graphene RF technology development.

3. Conclusions

Fig. 8 shows some important milestones that have been achieved in the past couple years. Although graphene technology development is still at its early stage, and many challenges remain to be solved to unleash its full potential, these fast progresses show certain promise of using it for future high-performance electronics.

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