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Top-gated graphene FET with Y_2O_3 for quantum capacitance estimation

Kosuke Nagashio, Tomonori Nishimura and Akira Toriumi
Department of Materials Engineering, The University of Tokyo
7-3-1 Hongo, Bunkyo, Tokyo 113-8656, Japan
Phone & Fax: +81-3-5841-1907, E-mail: nagashio@material.t.u-tokyo.ac.jp

1. Introduction

The Field effect by parallel palate capacitor is the heart of modern electronics. For low dimensional systems with low density of states, however, the situation is not so simple, since the energy cost of moving charge is considerably large. The contribution of this "self capacitance" (so-called quantum capacitance (C_Q)) to the total capacitance (C_{total}) should be taken into account, since the gate controllability is considerably weakened [1].

In order to extract C_Q of graphene with high accuracy, it is necessary to increase the contribution of C_Q in C_{total} by using the thin high-k topgate insulator. Recently, oxidation of Y on graphene has been reported to be effective to fabricate thin high-k insulator without the leakage current [2]. In this study, in order to improve the quality of Y_2O_3, Y_2O_3 was deposited on graphene in O_2 ambient without any damage by low energy process. The objective of this study is to extract the quantum capacitance of graphene by the capacitance measurement.

2.1 Selection & Characterization of Y_2O_3 insulator

The strategy to fabricate high quality high-k insulator on graphene is the deposition of metal with high oxidation ability in O_2 ambient. The oxidation ability of Y is the highest in the high-k materials and also higher than that of C based on the standard Gibbs free energy changes for oxidation. Therefore, it is expected that Y_2O_3 is thermodynamically stable on graphene.

In order to optimize O_2 partial pressure (P_{O2}) during Y_2O_3 deposition, Y with ~3 mg was thermally evaporated on p-Si by the resistive heating in controlled P_{O2}. Then, the capacitance measurement of MOS structure (Au/Y_2O_3/Si) was carried out, as shown by the inset in **Fig. 1(b)**. **Table 1** shows the summary of physical and electrical properties of Y_2O_3 insulator deposited at different P_{O2}. The best condition was found at $P_{O2}=10^{-1}$ Pa.

Table 1 Physical & electrical properties of Y_2O_3 on Si.

O_2 pressure [Pa]		< 10^{-4}	10^{-3}	10^{-2}	10^{-1}	10^{0}	10^{1}
	thickness [nm]	6.1	6.9	5.3	5.1	3.0	2.7
	RMS [nm]				0.36	0.33	0.45
As-depo.	C_{ox} @ 1MHz					0.7	×
	Jg @1V					10^{-6}	10^{-3}
	Breakdown V					3.3	2.8
Annealed*	C_{ox} @ 1MHz	×	×	0.6	0.6	0.6	×
	Jg @1V			5×10^{-7}	10^{-7}	10^{-7}	-
	Breakdown V			4.6	6	4~6	-

*Annealed condition: 200C 100%O_2 10 min + 300 C 0.1%O_2 30s

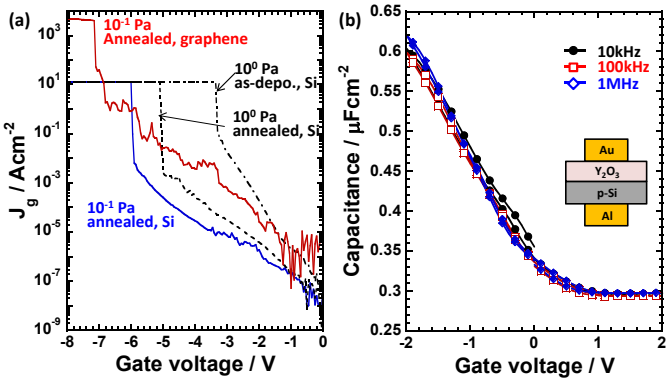

Fig.1 (a) Leakage current of Y_2O_3, (b) bidirectional CV curve of MOS capacitor.

At the lower and higher P_{O2} conditions, the capacitance was not measured due to the large leakage.

Figure 1(a) shows the leakage current for different conditions. Although adequate leakage current and breakdown voltage were not achieved for as-deposition, the combined low temperature annealing at 200 °C and 300 °C was effective to reduce the leakage current. **Figure 1(b)** shows bidirectional CV curves at different frequencies. Small frequency dispersion indicates that the degree of oxidation is high enough for the top gate insulator, which is considered to result from the high oxidation ability of Y. The dielectric constant is estimated to be 4.1 by using the thickness of 5.1 nm determined by grazing incidence X-ray reflective technique.

Finally, it should be emphasized that the Raman D band was not observed even after Y_2O_3 was deposited on graphene transferred on SiO_2/Si wafer and annealed in the determined conditions.

2.2 Y_2O_3 topgate modulation

Graphene was transferred by mechanical exfoliation of Kish graphite on SiO_2/n^+-Si wafer which was annealed at 1000 °C for 5 min in O_2 ambient as the pre-surface treatment. The source and drain electrode (Ni/Au) were fabricated by conventional electron beam lithography technique. Y_2O_3 was deposited on the whole area of wafer at $P_{O2}=10^{-1}$ Pa and annealed at 200 °C for 10 min. in O_2 gas flow. The top gate electrode (Ni) was fabricated again by EB lithography. Finally, the device was annealed at 300 °C for 30 s in 0.1 %O_2 before the electrical measurement in vacuum probe station. The image of typical topgate device is shown as the inset in **Figure 2(b)**.

Figure 2(a) shows the drain current as a function of

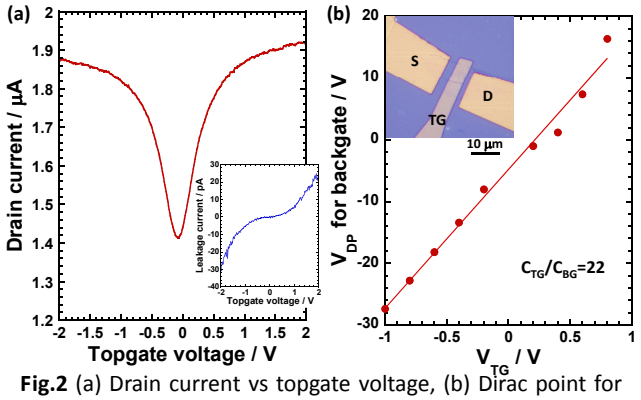

Fig.2 (a) Drain current vs topgate voltage, (b) Dirac point for backgate sweep at different V_{TG}.

Table 2 Comparison of gate oxide capacitance.

group	Material	Method	C_{ox} μF/cm²	Ref.
Manchester	Al_2O_3	Depo. in O_2	0.47	[3]
UT, Austin	Al_2O_3	ALD	0.74	[4]
NIMS	Al_2O_3	Air oxidation	1.0	[5]
IBM	HfO_2	ALD	0.41	[6]
IBM	SiN	CVD	0.68	[7]
Columbia	BN	exfoliation	0.34	[8]
Pekin	Y_2O_3	Air anneal	1.46	[9]
This work	Y_2O_3	Depo. in O_2	0.86	

top gate voltage (V_{TG}). The typical ambipolar behavior was observed. The leakage current is the order of pA even though the thickness of Y_2O_3 is ~5nm. The breakdown voltage was relatively high, as shown in **Fig. 1(a)**. The field effect mobility, which include the contact resistance and the resistance of access region (no-gate controlled), was estimated to be ~830 cm^2/Vs at the carrier density of 10^{12} cm^{-2}.

When the backgate voltage (V_{BG}) is swept at different V_{TG}, Dirac point continuously shifts. This is understood by electrostatic "doping" by the top gate. **Figure 2(b)** shows Dirac point voltage determined by the backgate sweep as a function of V_{TG}. Based on the capacitive equivalent circuit, the shift of Dirac point is related with the ratio of topgate and backgate capacitance as

$$\Delta V_{DP} = \frac{C_{Y2O3}}{C_{SiO2}} \times \Delta V_{TG} . \qquad (1)$$

Therefore, C_{Y2O3} can be determined as 0.86 μF/cm² since the slope is 22 (=C_{TG}/C_{BG}). This value is relatively large, compared with those of other top gate insulators reported so far, as shown in **Table 2**. For the case of thin gate insulator, the contribution of C_Q to the topgate total capacitance is large. However, it should be emphasized that C_{Y2O3} can be obtained in this analysis since C_Q is zero at Dirac point.

2.3 Quantum capacitance measurement

Finally, the total topgate capacitance is shown in **Fig. 3(a)**. This strong V_{TG} dependence indicates the contribution of C_Q. The measured capacitance is modeled as the inset in **Fig. 3(a)**, where C_{para} is parasitic capacitance. In order to extract quantum capacitance, C_{Y2O3} and C_{para} were adjusted to be 0.59 and 0.2 μF/cm² as fitting parameters, respectively. Fitted curve is shown as solid line in **Fig. 3(a)**. **Figure 3(b)** shows the estimated C_Q of graphene, where only positive topgate voltage side in **Fig. 3(a)** is considered. The solid red line is the theoretical prediction of C_Q as [1]

$$C_Q = e^2 DOS(E_F) = 2e^2 \frac{E_F}{\pi (v_F \hbar)^2} . \qquad (2)$$

For E_F>0.15 eV, linear relation that resulted from linear DOS relation is clearly observed, which cannot be proved by the transport measurement. Although the deviation from the theoretical curve near the Dirac point is considered due to the charged impurity, this behavior should be studied further.

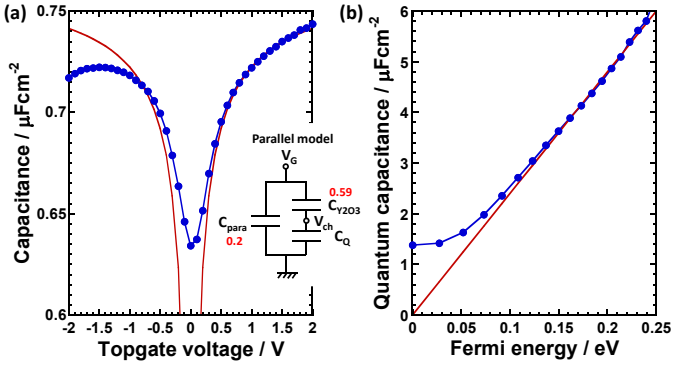

Fig.3 (a) Total topgate capacitance vs V_{TG}, (b) Estimated C_Q with theoretically predicted C_Q (solid line).

3. Conclusions

The high quality thin Y_2O_3 topgate insulator was fabricated by the thermal evaporation of Y in O_2 ambient and subsequent low temperature annealing process. Relatively high C_{Y2O3} value enabled us to extract C_Q and to observe linear relation of DOS as a function of E_F.

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References

[1] T. Fang, et al., APL, 2007, **91**, 092109.
[2] Z. Wang, et al., Nano lett., 2010, **10**, 2024.
[3] L. A. Ponomarenko, et al., PRL, 2010, **105**, 136801.
[4] B. Fallahazad, et al., APL, 2012, **100**, 093112.
[5] H. Miyazaki, et al., Nano lett., 2010, **10**, 3888.
[6] F. Xia, et al., Nano Lett., 2010, **10**, 715.
[7] W. Zhu, et al., Nano lett., 2010, **10**, 3572.
[8] A. F. Young, et al., arXiv:1004.5556v2 (2010).
[9] H. Xu, et al., APL, 2011, **98**, 133122.