Growth of High-Quality h-BN Nanosheets for Graphene Electronics

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1. Introduction

Hexagonal boron nitride (h-BN) has received a great deal of attention as a substrate material for high-performance graphene electronics, because it has an atomically smooth surface without dangling bonds and charge traps, similar lattice constant to that of graphene, large optical phonon modes, and a large electrical band gap (~5.9 eV) [1-2]. However, h-BN monolayers are generally produced by the micromechanical cleavage of a bulk h-BN crystal, which is limited to small sizes and suitable techniques [3]. For practical applications, the realization of high-quality and large-area h-BN consisting a homogeneous monolayer of a few layers is essential.

Recently, reproducible and scalable chemical vapor deposition (CVD) processes for fabricating few-layer h-BN films on transition metal surfaces have been reported [4-5]. Although large-area few-layer h-BN films have been successfully realized using the CVD process, there are still many issues which remain to be resolved, including the formation of defects such as allotropes and impurity particles on the h-BN surface.

Herein, we demonstrate a facile method of growing large-scale high-quality h-BN nanosheets by controlling the surface morphology of copper (Cu) foils acting as a catalyst. Furthermore, we characterize for the first time the electrical properties of large-scale CVD-grown graphene on CVD-grown h-BN nanosheets.

2. Experiment and Results

Experiment

The synthesis of h-BN layers was carried out in an ambient pressure CVD system as described in a previous work [4]. For the growth process, a Cu foil was placed in the CVD chamber and gradually heated up to 1000 ℃ in a mixed Ar/H_2. Then, the main growth was carried out in a mixed Ar/H_2 gas for 30 min at 1000 ℃ with ammonia borane (NH_3-BH_3) as the source material sublimated at 110-130 ℃ using a subheating chamber with an N_2 gas. After the synthesis, the nanosheets were transferred to arbitrary substrate for further characterization and device fabrication as reported in graphene transfers [6].

The surface roughness of nanosheets measured by atomic force microscopy (AFM) in tapping mode provides further insight into the degree of uniformity. The BN structures were characterized by Raman spectroscopy. To confirm the reliability of the h-BN nanosheets for device applications, a graphene FET was fabricated in a similar manner to that in a previous report based on the mechanical cleavage of graphene and h-BN [7]. To control the surface morphology of the Cu foil, we introduced two methods (thermal annealing (TA) and thermal annealing/chemical polishing (TA/CP)).

Results and discussion

The untreated Cu foil with small grains having a size of ~30 μm was changed to flat Cu foil with large grains having a size of ~120 μm size after thermal annealing at 1020 ℃, as shown in Figure 1a,b. The flat surface morphology of the TA/CP-treated Cu foil was made by rubbing with Cu etchant after thermal annealing, as shown in Figure 1c. The surface roughness was measured by AFM which was gradually smooth after treatment. The insets of Figure 1a-c show the schematic illustrations of the morphology-controlled Cu foils. The h-BN nanosheets grown on the Cu foils were transferred onto SiO_2/Si wafer as shown in Figure 1d-f. The number of impurity particles in the h-BN nanosheets slightly decreased as compared to that in the h-BN nanosheets grown on the untreated Cu foil (Figure 1d,e). Moreover, the formation of impurity nanoparticles in the h-BN nanosheets grown on the TA/CP treated Cu foil is dramatically suppressed (Figure 1f), resulting in large-area nanosheets with an atomically flat surface roughness.

The AFM images over an area of 1 $\times$ 1 μm^2 are shown insets of Figure 1d-f. The h-BN nanosheets grown on the untreated Cu foil have a rough surface morphology with an rms roughness of 2.42 nm. The h-BN nanosheets grown on the TA-treated Cu foil are slightly smoother with an rams roughness of less than 1.57 nm. On the other hand, the surface rms roughness of the h-BN nanosheets grown on the TA/CP-treated Cu foil is 1.10nm. These results suggest that the flat surface and large grain size of the catalyst layer are essential to suppress the formation of impurity nanoparticles in the h-BN nanosheets.

Figure 2a shows the I_{ds}-V_g characteristics of FETs fabricated using two-type graphene structures: one with the h-BN nanosheets obtained from the TA/CP-treated Cu foil and the other without the h-BN nanosheets. Each device has a L of 10 μm and W of 2 μm. The transfer curves

measured under ambient conditions show p-type behavior. The Dirac point of the graphene device with the high-1uality h-BN nanosheets is downshifted to $V_g = 13$ V as compared to that of the graphene device without h-BN, which is observed at $V_g = 20$ V. In addition, the on-off ratio of the I_{ds} of the graphene device with the h-BN nanosheets is 2 times higher than that of the graphene device without the h-BN nanosheets. As shown in Figure 2b, the hole mobility of graphene assisted by the h-BN nanosheeets is 3-fold higher (~573 cm^2 V^{-1} s^{-1} at - 2 $\times$ 10^{11} / cm^2) than that of graphene on SiO2 (~199 cm^2 V^{-1} s^{-1} at - 2 $\times$ 10^{11}/ cm^2).
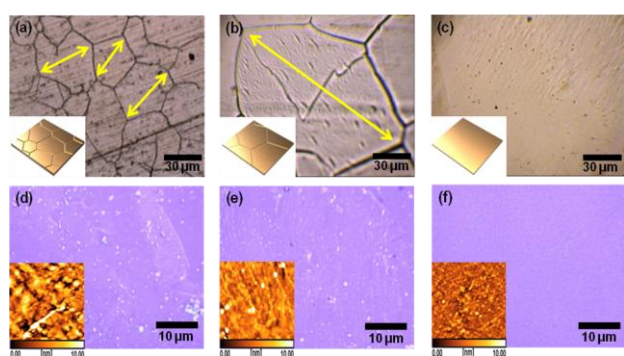

Fig. 1 Optical image of Cu foil by (a) no treatment (b) thermal treatment at 1020 oC for 2hr (c) chemical polishing after thermal treatment. Inset of (a~c) show the schematic illustrations for morphologhy control of Cu foil. Optical image of h-BN on SiO2 after growth on (d) no treated Cu foil (e) thermal treated Cu foil (f) chemical polishing Cu foil after thermal annealing. Inset of (d~f) show the corresponding AFM images (scan area is 1 x 1 μm).
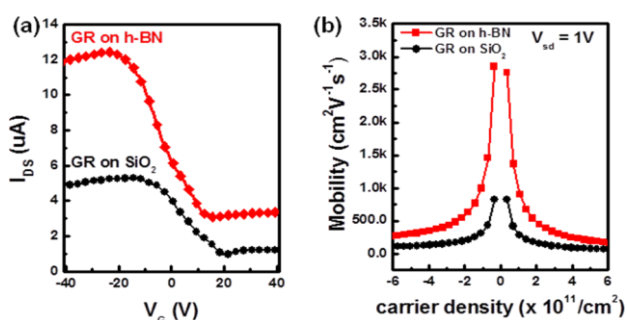

Fig. 2 (a) I_{ds}-V_g characteristics of graphene (GR) TFTs on bare SiO$_2$ and high-quality h-BN nanosheets in atmospheric ambient. The inset is an optical image of the TFT arrays. (b) Mobility as a function of charge carrier density in graphene.

3. Conclusions

We studied the influence of the Cu morphology on the high-quality growth of h-BN nanosheets. The number of impurity particles on the h-BN nanosheets and roughness of the Cu foil were strongly dependent on whether the Cu substrate was subjected to thermal annealing and chemical polishing or not. For the first time, the performance of large-area graphene devices based on high-quality h-BN nanosheets grown using the CVD approach was investigated, and a 3-fold higher mobility and on/off ratio were achieved. We expect that our approach can provide a beneficial method of preparing high-quality h-BN nanosheets to be utilized in high-performance large-area graphene electronics in the future.

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