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Graphene ReRAM towards All Graphene LSIs: Experimental Demonstration of Two-terminal ReRAM Operation in Electrically Broken Mono- and Multi-layer Graphene

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1. Introduction

Thanks to outstanding electrical and thermal properties, graphene offers potential to be a new material for future nanoscale electronic devices. A number of researchers have reported the applications of graphene to FETs [1], interconnects [2], and diodes [3]. Although breakdown characteristics are very important for these applications, breakdown mechanisms nor post-breakdown graphene characteristics have not yet been fully investigated.

In this study, we found that two-terminal graphene devices on SiO_2 show ReRAM characteristics after electrical breakdown. Although nonvolatile memory effect in graphene FETs [4] and graphene oxide memory [5] have been reported, this is the first demonstration of graphene ReRAM. The realization of graphene ReRAM may open a way to memory-embedded graphene interconnects and transparent, flexible graphene SoCs consisting only of graphene devices and components.

2. Device Structure

Fig. 1a shows the structures of exfoliated graphene devices used in this work. Ti/Au or Cr/Au is used as the contact metal. The layer number of graphene is eight for Ti/Au devices; one or six for Cr/Au devices. Fig. 1b shows sheet resistance versus gate voltage (V_g) characteristics of mono- and multi-layer devices, demonstrating successful, ideal operation of graphene FETs. All the electrical characteristics were measured in the vacuum chamber at the base pressure of lower than 10^{-2} Pa.

3. Results and Discussion

A. Electrical breakdown of graphene

Fig. 2 shows the drain current (I_d) versus drain voltage (V_d) characteristics of a fresh graphene device. It is clearly shown that the graphene is electrically broken at the V_d of 3.7 V. After the breakdown, extremely small I_d is observed even when the V_d is increased to 5 V.

However, the resistance of the broken graphene is suddenly and greatly reduced when V_d is swept from 0 V to a write voltage (V_w) as shown in Fig. 3. This sweep defines a write operation that changes the device resistance sate from HRS (High Resistance State) LRS (Low Resistance State). Fig. 3 also shows the erase operation that switches the device state from LRS to HRS when V_d is increased to an erase voltage (V_e). These write and erase operations constitute the ReRAM operation in the broken graphene.

B. Broken graphene properties as ReRAM

Next, the properties of the broken graphene as ReRAM are obtained. Fig. 4 shows the retention characteristics, demonstrating the high HRS/LRS ratio of about 10^6 and long retention time of greater than 10^3 seconds. Fig. 5 shows the endurance characteristics, indicating the resistance ratio between HRS and LRS is kept greater than 10^3 during the 10^3 cycle.

Fig. 6 shows the time evolution of I_d and V_d during a write operation, where V_d is changed from the read voltage (V_r) of 1V to V_w of 4V. In this measurement, the sampling rate was 10 ns, which was the finest resolution of the present instrument. I_d is increased to a value 10^3 times greater than I_d in HRS at 300 ns later after the write pulse edge. Fig. 7 represents HRS resistance as a function of erase pulse width. At each erase pulse width, the erase operation was performed ten times. Fig 7 clearly shows that the erase operation was successfully performed even with the shortest erase pulse width of 10 ns. Shorter pulse widths lead to higher HRS resistances with a tighter distribution. The shortest time of 10 ns means that the fastest switching occur within 30 ns including the 10-ns rise and fall slopes of the pulse. It should be noted that this is the shortest pulse limited by our present equipment.

C. Width dependence of graphene ReRAM property

Considering the application for LSI, the device scaling is very important. Channel width (W) dependences are studied in Fig. 8. Wider W results in an increased I_d as well as a reduced V_e during the erase operation (Fig. 8a). Fig. 8b shows that I_d during reading decreases in narrower W. In terms of energy, the erase operation consumes much higher energy than the write operation. Fig. 8c shows the erase energy as a function of W, demonstrating that the erase energy is lower for smaller W and it takes the lowest value of 24 pJ with W of 30 nm. Both the read power consumption and erase energy decrease with a narrower W.

D. Operation principles of graphene ReRAM

So far, the ReRAM effect has been observed in the Cr/Au device. However, this effect is also confirmed in Ti/Au device (Fig. 9). Because ReRAM effect has no dependence on the type of the contact metal, we consider that the ReRAM mechanism in the present system has no relationship with graphene/electrode interface. This prospect is supported by Fig. 10, where the AFM image of graphene channel before and after the breakdown is shown. The initial graphene channel shows FET characteristics as shown in Fig. 1b. After the breakdown, the disconnected area appeared in the channel (Fig 10b), indicating that the origin of turning graphene to HRS are obviously in the graphene itself. One possible mechanism is structural changes of graphene in atomic scale; change between the original sp^2-bonded state with higher conductivity and the sp^3-bonded state with lower conductivity [6]. Another possibility is interactions between graphene and SiO_2. This expectation is supported from the fact that the disconnected area of graphene forms a groove in SiO_2. Interactions among different layers of multilayer graphene are less plausible because the ReRAM effect is observed also in the monolayer graphene (Fig. 11).

4. Conclusions

Mono- and multi-layer graphene ReRAM are experimentally demonstrated. Electrically broken graphene recovers conductivity by applying an appropriate V_d and shows good ReRAM characteristics. The switching energy decreases with a decrease in W, indicating suitability of graphene ReRAM for high-density LSI memory. It is expected that the origin is structural changes of graphene in atomic level or interactions between graphene and SiO_2.

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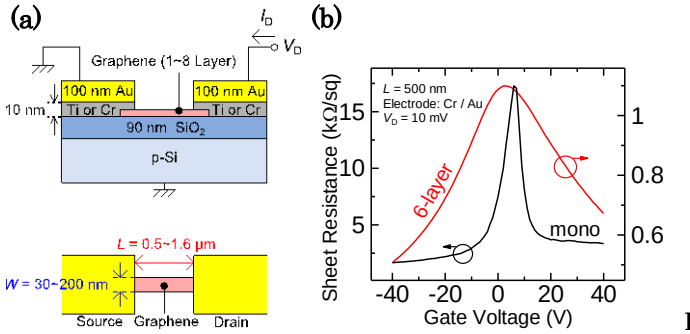

Fig. 1: (a) Schematic of device structure. **(b)** Sheet resistance (R_s) as a function of gate voltage (V_g). Typical $R_s - V_g$ characteristics for monolayer and 6-layer graphene are obtained at drain voltage (V_d) of 10 mV.

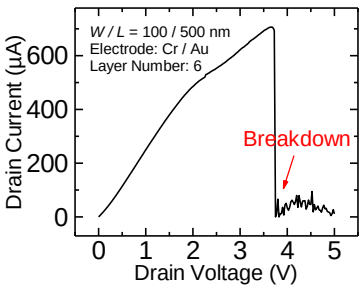

Fig. 2: Breakdown characteristics of 6-layer graphene device. The device is electrically broken at the power of 2.6 mW.

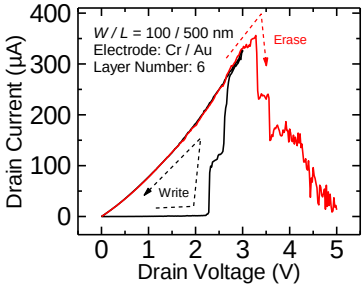

Fig. 3: $I_d - V_d$ characteristics for write and erase operations. After writing, the resistance of graphene is recovered to an about half value of its initial resistance.

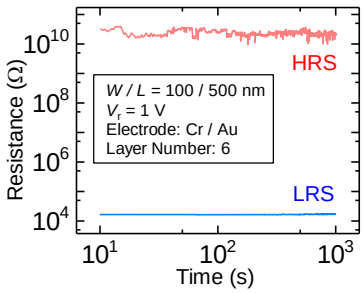

Fig. 4: Retention characteristics. Long retention of 10^3 seconds for both HRS and LRS is observed at a read voltage (*Vr*) of 1 V at 300 K.

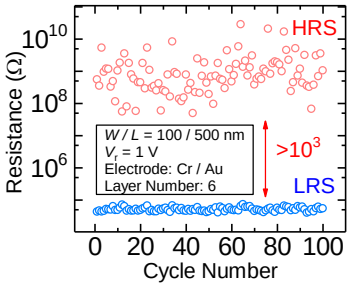

Fig. 5: Endurance characteristics. Endurance is confirmed for 10^2 cycles at read voltage (*Vr*) of 1 V. On/Off ratio is kept greater than 10^3 during this measurement.

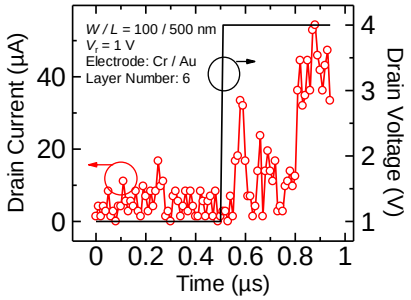

Fig. 6: Write characteristics. The resistance change is occurred 300 ns later after applying write pulse.

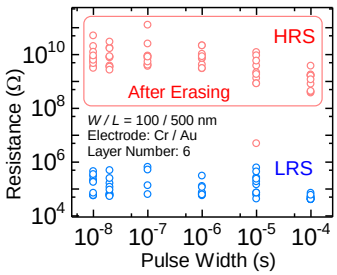

Fig. 7: Erase characteristics as a function of erase pulse width. Shorter erase pulse widths lead to better HRS resistances. The HRS resistances are obtained 10 times at each pulse width. The shortest width of 10^{-8} s is the limit of the instruments.

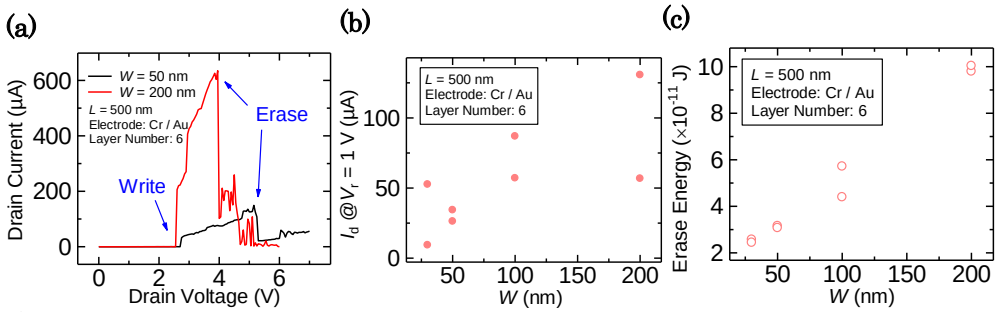

Fig. 8: (a) Channel width (*W*) dependence of switching characteristics. A wider channel requires higher current for erase operation. However, it switches at a lower voltage. **(b)** *W* dependence of LRS I_d. Better conductivity is obtained for larger *W*. **(c)** Erase energy as a function of *W* at the erase time of 40 ns. The energy for erase operation gets smaller at narrower *W*, indicating scalability of the present graphene ReRAM.

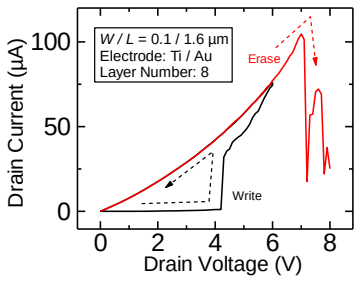

Fig. 9: Write and erase operation for devices with Ti/Au electrode. Electrodes with a different material show basically the same ReRAM effect, which means that the interface of graphene and electrode is not the origin of graphene ReRAM.

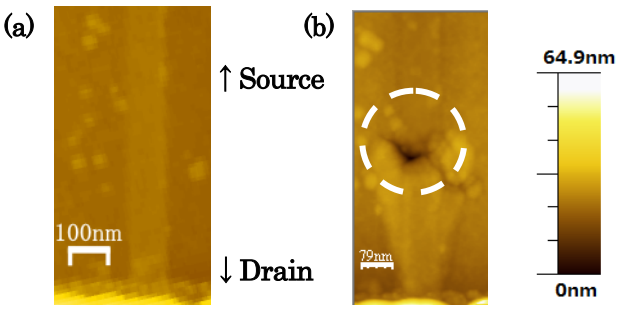

Fig. 10: (a) AFM image of initial graphene channel. It is confirmed that (before the breakdown) this graphene works as FET. **(b)** AFM image of HRS graphene channel after the breakdown. A disconnected area exists in the graphene, indicating that ReRAM effect takes place in graphene channel. Moreover, this disconnected area forms a groove in SiO_2. This fact suggests that there are interactions between graphene and SiO_2.

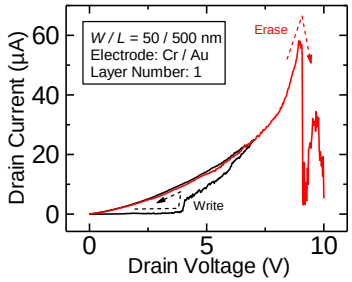

Fig. 11: Write and erase operation of monolayer device. ReRAM effect is observed also in monolayer graphene. Therefore, an inter-layer reaction is not an operation principle.