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Epitaxial Graphene: Synthesis, Integration, and Nanoscale Devices

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1. Introduction

Scaling theory predicts that a field effect transistor (FET) with a thin barrier and a thin gate-controlled region will be robust against short-channel effects down to very short gate lengths. Graphene, a monolayer of carbon atoms tightly packed into a two-dimensional (2D) honeycomb lattice, is the ultimate thin-body semiconductor and thus exhibits unmatched electrostatics.[1 , 2] Impressively, state-of-the-art graphene-based transistors have been shown to operate at >400 GHz when utilizing self-aligned device architectures.[3][4] In fact, recent reports have shown the potential for exfoliated,[5] chemical vapor deposited,[6] and epitaxial graphene[7] to exceed frequency performance of Si-MOSFET technology. Graphene derived from silicon carbide (SiC) – referred to as epitaxial graphene – has proven to be an excellent material system for high frequency electronic applications.[7] However, simple utilization of graphene as a channel material in field effect transistors does not guarantee high frequency device performance. Essential to the development of ultra-thin body devices based on graphene is the integration of graphene with high purity metals and ultra-thin dielectric materials. In order to achieve state-of-the-art graphene technologies, one must address several key features in material and device development: graphene carrier transport, Ohmic contact resistance, dielectric integration, and device scaling.

2. Experimental Methods

Epitaxial graphene (EG_{Si}) is synthesized via silicon sublimation from SiC(0001) at 1625 ^{o}C, for 15 min at 1 - 200 torr. Following synthesis, epitaxial graphene is characterized via Raman spectroscopy, x-ray photoelectron spectroscopy (XPS), and Lehighton non-contact mobility and sheet resistance (LEI,Inc). Raman confirms the successful growth of monolayer EG_{Si} on the SiC(0001) terrace and bilayer EG_{Si} on the terrace step edge.[8,9] Subsequently, samples undergo exposure to molecular hydrogen (H_2) at 600 – 1200 ^{o}C, 600 Torr for 30 – 120 min (referred to as hydrogen intercalation). This process results in quasi-free standing epixatial graphene (QFEG). Device processing utilizes standard photolithographic techniques. Integration of a gate dielectric with graphene is comprised of various steps, with ALD and EBPVD being utilized to prepare either EBPVD or EBPVD seeded ALD films. EBPVD seeded ALD dielectrics utilize a ~2 – 3 nm seed layer of SiO_2, Al_2O_3, or HfO_2 deposited via non-reactive EBPVD at < 10^{-6} Torr. Immediately following EBPVD seeding, ~8 – 10 nm of Al_2O_3 or HfO_2 is deposited via ALD (Cambridge Nanotech, Inc "Savannah") to complete the gate stack. Source/drain spacings in the graphene FETs are 750 nm for "traditional" samples and 75 nm wider than the gate length for scaled devices (i.e. for 75 nm gate length, S/D spacing is 150 nm). Gate lengths evaluated in this work are 1000, 750, 250, and 75 nm, where 250 and 75 nm gate lengths represent scaled devices.

3. Results & Discussion

SiC substrates used in this work have a nominal miscut of zero degrees from the (0001) crystal axis, but existence of a slight miscut leads to a terraced morphology (Figure 1a). Due to the unique growth kinetics present at the step-edge, graphene nucleation and subsequent growth occur rapidly, leading to multi-layer graphene at the step edge with bilayer on the terrace surface (Figure 1b).[10] We find that that not only are step edges a source of additional scattering, but that they also lead to an increase in hole doping. Temperature dependent Hall measurements indicate an increase in remote charged impurity scattering and remote surface optical phonon scattering for high step-edge density samples. Hydrogen passivation of EG_{Si} results in a reduction of impurity scattering, attributed to the passivation of defects and dangling bonds at the graphene-SiC interface after hydrogen intercalation. Importantly, for the QFEG samples it is found that there is an additional reduction in impurities by moving from a high step-edge density sample to one with low step-density. Thus, reducing the step-edge density leads directly to a reduction in charged impurities and, subsequently, remote charged impurity scattering and enhanced mobility.

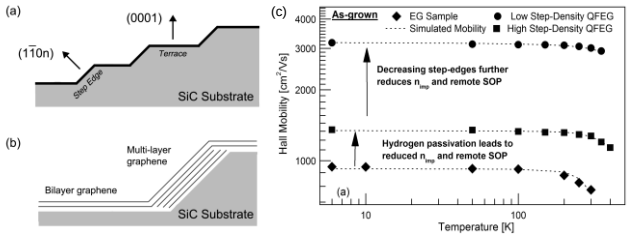

Figure 1: (a) Schematic of SiC surface before and (b) after high temperature graphitization and hydrogen passivation illustrating significant step-bunching in the substrate. (c) Plot comparing as-grown EG_{Si} to high and low step-density QFEG samples, indicating that step edges are a likely source of both scattering processes.

To achieve superior high frequency performance, device scaling requires ohmic contacts to exhibit a specific contact resistance < $1x10^{-9}$ Ω-cm^2. We have developed a robust method for forming high quality ohmic contacts to graphene, which improves the contact resistance by nearly

6000x compared to untreated metal/graphene interfaces. Optimal specific contact resistance for treated Ti/Au contacts is found to average < 100 Ohm-µm. Additionally, we examine Al/Au, Ti/Au, Ni/Au, Cu/Au, Pt/Au, and Pd/Au contact metallizations, and find most metallizations result in similar specific contact resistances in this work, regardless of the work function difference between graphene and the metal overlayer. Table two summarizes the current work and compares it to other work on similar graphene.

Table 1: Contact Resistances for current work compared to literature values on EG_{Si} and QFEG.[11]

Work	R_c [ohm-µm]	Mobility [cm²/Vsec]	N_{sh} [cm⁻³]	R_{sh} VdP [ohm/square]
PSU [Pd/Au]	121	900-2000	1e13	333-840
PSU [Ti/Au]	67.9	900-2000	1e13	333-840
HRL [EG]	20-80	860-1250	1e13	-
HRL [QFEG]	60-80	2500	7e12	232-283

In addition to low resistance ohmic contacts to graphene, a key limitation to the realization of graphene's full potential comes from its interaction with dielectric interfaces, which can degrade the excellent charge transport properties of graphene. Typically, top-gated graphene field effect transistors are fabricated with one of various high-k gate dielectrics. We have successfully utilized atomic layer deposition of high-k dielectrics to not only improve graphene transport, but also produced high performance graphene transistors when implemented with QFEG.[12][13] Additionally, we have recently developed methods to integrate hexagonal boron nitride with graphene to enhance the transport and device performance compared to HfO_2. Figure 2 summarizes the results of this effort. Although the integration of HfO_2 and h-BN with high step-edge density QFEG shows relatively little gain in performance when utilizing h-BN, low step-edge density QFEG benefits significantly with a ~2.6x increase in Hall mobility to values >3000 cm^2/Vs, emphasizing that the overall benefit of h-BN dielectrics is dependent on the effective remote charged impurity density.

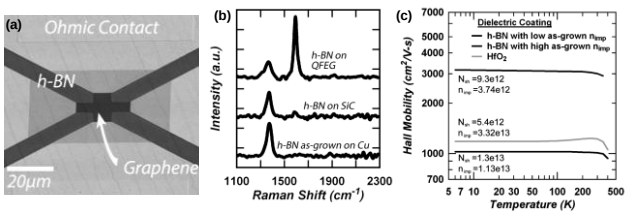

Figure 2. (a) Quasi free-standing epitaxial graphene hall cross upon which h-BN is transferred and subsequently patterned. (b) Raman spectra of as-grown h-BN on the copper substrate compared to transferred h-BN on a SiC substrate and over QFEG, and (c) Hall mobility versus temperature shows the potential of h-BN in preserving high mobilities for QFEG as well as its reduced introduction of remote surface optical phonon scattering at higher temperatures compared to HfO_2. Here, N_{sh} is the sheet carrier density (cm^{-2}).

Radio-frequency performance for h-BN gated GFETs is highly dependent on the impurity density of the dielectric-QFEG system. Figure 3a is an SEM image of a RF transistor utilizing hBN, and Figure 3b plots the small signal current gain for three different GFETs as a function of frequency after de-embedding the pad parasitics using a short-open-load-thru compensation. The h-BN gated QFEG sample having a high impurity density and the HfO_2 gated QFEG sample exhibit a current gain cutoff frequency (f_T) of 5.4 GHz and 13.8 GHz, respectively; indicating that at high impurity densities, h-BN has no benefit over HfO_2 in the Coulombic scattering dominated regime due to dielectric screening. Alternatively, for the h-BN gated QFEG sample with a low impurity density, the intrinsic cutoff frequency was measured to be 33.5 GHz ($f_T \cdot L_g$ = 25.12 GHz-um). The dramatic 2.4x increase in f_T over the HfO_2 coated sample is attributed to h-BN's high energy phonon modes benefiting from the increased contribution to the overall scattering rate from remote surface optical phonon scattering in the low impurity regime.

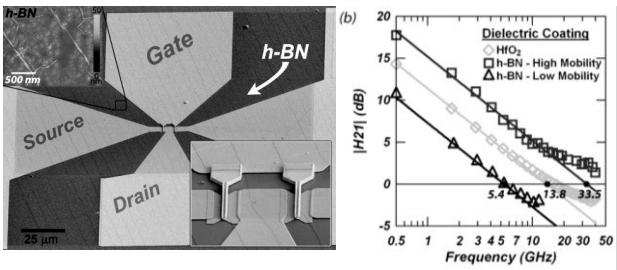

Figure 3: (a) FESEM image of an h-BN gated FET structure. (b) Intrinsic RF performance for h-BN gated devices with high and low impurity densities compare to an HfO_2 gated device.

4. Conclusions

We have developed means to synthesize epitaxial graphene with excellent carrier mobilities (>3000 cm^2/Vs), integrate this graphene with high quality metals and dielectrics while preserving transport properties; and have produced high performance graphene devices with $f_T \cdot L_g$ products >25 µm-GHz.

Acknowledgements

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