

Ultimate Scaling of High-k Gate Dielectrics: Current Status and Challenges

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1. Introduction

Continued CMOS device scaling for the 22 nm node and beyond requires sub-nm EOT to suppress short-channel effects. A typical high-k dielectric and metal electrode stack structure contains a SiO₂-based interfacial layer (IL), a high-k dielectric, followed by a metal gate electrode. EOT scaling is possible with the following three approaches: (1) Introduce a new high-k material with k-value greater than that of HfO₂ (higher-k); (2) Increase the k-value of IL; (3) Reduce the physical thickness of IL. In this paper, we review current status and challenges for each approach and discuss the EOT scaling strategy for future CMOS devices.

2. Higher-k Materials

Table I summarizes recently reported IL k-boost and higher-k data. EOT values less than 0.80 nm have been achieved with both approaches, however, the aggressive scaling is accompanied with effective workfunction (EWF) shift toward the Si conduction band minimum (CBM) in most cases. This trend makes application of these materials to pFET extremely difficult. Development of pFET compatible higher-k materials is one of the biggest challenges to overcome.

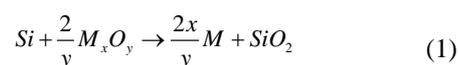
Table I Summary of IL k-boost and higher-k data in literature.

Materials	k-value	EOT (nm)	EWF with TiN
La-silicate IL [1, 2]	-	0.58-0.62	~ Si CBM
SrO IL [3, 4]	-	0.50-0.60	~ Si CBM
Y/Si doped HfO ₂ [5, 6]	27	-	-
La-Lu-O [7]	23	0.58	~ Si CBM
Y-La-Si-O [8]	-	0.77	~ Si CBM
La ₂ O ₃ [9]	-	0.62	~ Si CBM
La-Al-O [9, 10]	23-25	0.31-0.74	Si CBM ~ Si mid-gap

3. Interfacial Layer Scavenging Approach

IL scaling via scavenging reaction has become a mainstream approach in recent years to realize EOT 0.5 nm and less. Choice of scavenging element is one of the most important factors for IL scavenging reaction. We found that the Gibbs free energy change at 1,000 K ($\Delta G^\circ 1000$) of the following reaction (1) serves as a guiding principle for the

choice of scavenging element [11].



where M is the scavenging element in the gate stack. The EOT trend for metal-inserted poly-Si stack (MIPS) with SiO₂/HfO₂ dual-layer gate dielectrics in the literature is summarized in Fig. 1 as a function of $\Delta G^\circ 1000$ per oxygen atom ($\Delta G^\circ 1000/O$) for the scavenging element. As shown in Fig. 1, EOT and $\Delta G^\circ 1000/O$ values show a very strong correlation. We proposed doping of scavenging metals with high $\Delta G^\circ 1000/O$ values into a thermally stable TiN electrode. This technique enables highly controllable IL scavenging for both gate-first [1] and gate-last [12] integrations.

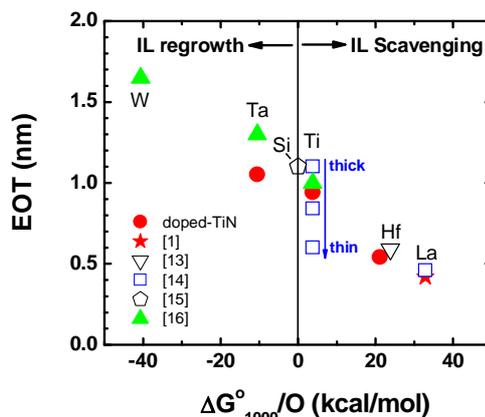


Fig. 1 EOT of SiO₂/HfO₂ MIPS structure as a function of $\Delta G^\circ 1000$ per oxygen atom for scavenging element (after [11]).

3. Impact on EWF/Reliability/Mobility

We used the remote IL scavenging technique to investigate the impact of EOT scaling on the EWF for gate-last process. Fig. 2 compares the EWF-EOT trends for the nWF and pWF metals. The nWF metal provides a completely flat EWF-EOT trend down to 0.6 nm. On the other hand, the pWF metal shows a flat trend down to EOT 0.8 nm and then exhibits a linear trade-off trend toward the mid-gap with further scaling. Degradation in film quality in the sub-monolayer IL regime may facilitate oxygen vacancy generation in the HfO₂ layer [17, 18] and/or the SiO₂ IL [19], resulting in the unfavorable EWF shift for pFET. Thus, leaving an ultra-thin and robust SiO₂ IL after scavenging is indispensable for EWF control.

We investigated impacts of remote IL scavenging on reliability [20]. The change in the device lifetimes, includ-

ing PBTI, NBTI, and TDDB, are estimated and summarized in Fig. 3. Note that the estimated lifetime trends for IL scaling are similar for gate-first and gate-last processes. The BTI lifetimes are predicted to decrease by 50-100 \times for every 0.1 nm of IL scaling. Drastic lifetime reductions also occur for TDDB. Therefore, calculated IL scaling considering reliability requirements is needed for future CMOS nodes.

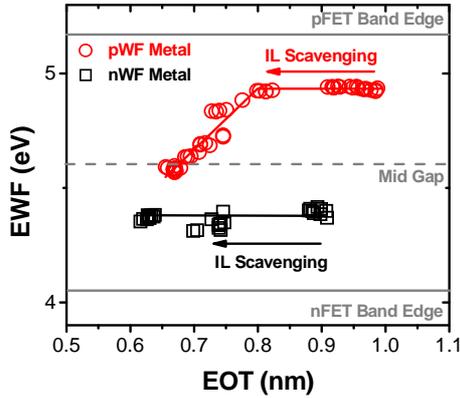


Fig. 2 EWF-EOT trend for pWF and nWF metals with gate-last process. The EOT was changed via remote IL scavenging technique (after [12]).

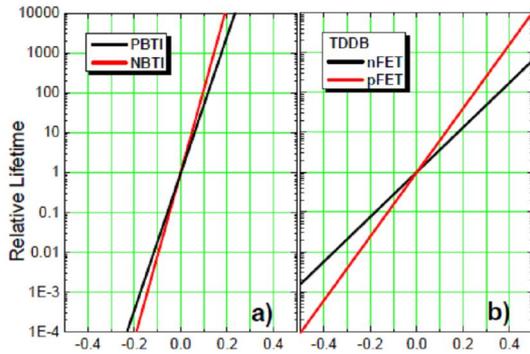


Fig. 3 Relative change of (a) PBTI and NBTI lifetime (b) TDDB lifetime for nFET and pFET with gate oxide thickness change via IL scavenging (after [20]).

Fig. 4 shows high field electron mobility as a function of EOT from literature data. The experimental data are compared with the estimated mobility-EOT relationship providing the same drive current (I_{on}) at a given L_g in [21]. The mobility-EOT slope for IL scavenging and La-silicate IL (~ 20 cm^2/Vs per 0.1 nm) is shallower than the estimated breakeven relationship for $L_g \leq 30$ nm (~ 40 cm^2/Vs per 0.1 nm). This indicates that it is indeed possible to improve the short-channel device performance by employing IL scaling in conjunction with aggressive L_g scaling in future nodes.

4. Conclusions

La-based higher-k materials and La-silicate IL with HfO_2 showed aggressive EOT values (0.5–0.8 nm), but with large EWF shifts toward the Si CBM, limiting their application to nFET. Further exploration for pFET-compatible higher-k materials is needed. Meanwhile,

IL scavenging is a promising approach to extend Hf-based high-k dielectrics to future nodes. Mobility-EOT trends in literature suggest that short-channel performance improvement is attainable with aggressive EOT scaling via IL scavenging or La-silicate formation. However, extreme IL scaling is accompanied with loss of EWF control and with severe penalty in reliability. Therefore, highly precise IL thickness control in an ultra-thin IL regime (<0.5 nm) will be the key technology to satisfy both performance and reliability requirements for future CMOS devices.

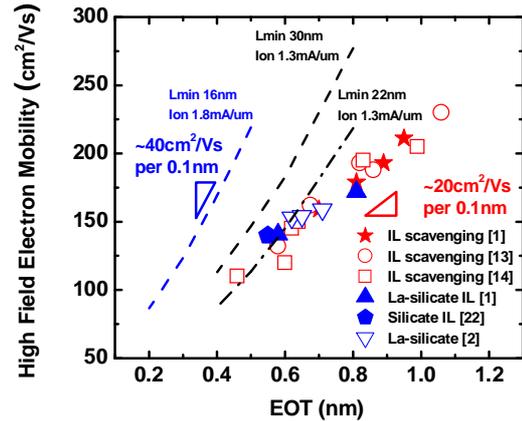


Fig. 4 High field electron mobility as a function of EOT from literature data [1, 2, 13, 14, 22]. The mobility values are taken at $N_{inv}=1 \times 10^{13}$ cm^{-2} in [14] and at $E_{eff}=1$ MV/cm in all other work. Simulated contour lines providing the same I_{on} at L_{min} 16, 22, and 30 nm [21] are shown for comparison (after [11]).

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