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Effective Work Function Engineering for Aggressively Scaled Planar and FinFET-based Devices with High-k Last Replacement Metal Gate Technology

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Abstract

We report on aggressively scaled RMG-HKL devices, exploring several options for effective work function (EWF) engineering and targeting logic high-performance and low-power applications. Planar devices with controlled TiN/(RF-PVD TiAl)-alloying show tight low-V_T NMOS distributions [$\sigma(V_{Tsat})$~49mV/(29mV for TiN-PMOS) at L_{gate}~35nm] using: 1) RF-PVD TiN with minimal sidewall deposition, to allow optimization of TiAl/TiN thicknesses at the bottom of gate trenches while maximizing the space to be filled with a low-resistance metal; or 2) ALD-TiN to avoid preferential paths, at gate sidewalls, for Al diffusion into the high-k, reducing J_G. For FinFETs, which require smaller EWF shifts for low-V_T: 1) conformal, lower-J_G ALD-TiN/TaSiAl; and 2) Al-rich ALD-TiN by controlled Al diffusion from Al fill-metal (in high aspect-ratio gates) are demonstrated to be promising candidates. Comparable BTI behavior, slightly reduced EOT and improved noise characteristics for Al-rich EWF-metal stacks are measured.

Introduction

Following successful implementation into devices manufacturing [1,2], high-k/metal gate faces key challenges on scalability towards ultra-thin EOT/T_{inv} with controlled effective work function (EWF), gate leakage (J_G), variability and reliability for (sub-)22nm technology nodes. For further CMOS scaling, FinFET-based multi-gate devices have long been considered an attractive option thanks to their improved electrostatics and reduced V_T variability due to lower channel doping [3]. Focus on these devices requires options compatible with their 3D-architecture which features gate control on three fin surfaces. In this work, we provide a comprehensive evaluation of EWF-metal alloying suitable for low-V_T NMOS scaled planar devices with both high-k and metal deposited last (RMG-HKL), addressing J_G reduction and minimized parasitic gate resistance. The latter is critical for circuits, with the devices built benchmarked on noise, reliability, and DC device performance. In addition, a thorough assessment of RMG-HKL options compatible with FinFETs is pursued, identifying potential conformal n-EWF metals (as-deposited or obtained through alloying).

Device fabrication

The process flow used for device fabrication is illustrated in Fig.1 [4,5]. Source/drain silicide is formed after RMG module, allowing introduction of higher thermal budgets during/after gate stack deposition. Fig.2 shows schematics of the RMG-HKL stacks evaluated in this work for n-EWF engineering (similar IL-SiO_2/HfO_2), using (ALD→CVD) W or HP-PVD Al (with a 400°C reflow and PVD-[TiN/Ti] or ALD-TaN/CVD-Co liners) as fill-metals.

Results & discussion

Al diffusion from TiAl into an underneath TiN layer was previously reported to result in low n-EWF values [4], with the amount of Al diffusing set by the TiAl/TiN thicknesses ratio and reduced by oxygen incorporation in the stack. In-situ [TiN/TiAl/TiN cap] and nitride-only spacers were therefore implemented to minimize oxygen sources during alloying. For scaled devices, with higher gate aspect-ratios (AR = L_{gate}-H_{gate}, W_{gate}-H_{gate}), it becomes increasingly difficult with PVD technology to maintain TiAl/TiN ratios for reduced L_{gate}. This is confirmed by the TEM and EDS images in Fig.3, which show thicker [TiN/TiAl/TiN] stacks at the bottom of gate trenches (H_{gate}~60-70nm) for larger devices (with lower AR), resulting in EWF control loss (higher V_T) for smaller L_{gate} (higher AR). Fig.4 shows that by reducing H_{gate} by up to 30nm and optimizing the TiAl/TiN ratio, improved control of layers thicknesses at the bottom of gate trenches (both in center and gate edges, L_{gate}≥35nm) can be achieved with RF-PVD. Strong Al signal is detected by EDS in small devices, in sharp contrast with the situation for the high AR devices in Fig.3. Tight low-V_T distributions down to small L_{gate} [$\sigma(V_{Tsat})$~49mV at L_{gate}~35nm] confirm good alloying control (Figs.4c,d). RF-PVD TiAl can be combined with RF-PVD TiN or ALD-TiN (Fig.5), each approach having its advantages: 1) minimal sidewall deposition with RF-PVD (highlighted by the TEM in Fig.4b) allows optimization of layers thicknesses at the bottom of trenches, while maximizing the space to be filled with a low-resistance metal (W or Al), hence minimizing gate resistance; 2) improved sidewall coverage with ALD-TiN means no preferential paths for Al diffusion, through TiN, into HfO_2 at gate sidewalls, resulting in the reduced J_G shown in Fig.6. Fig.7 shows normalized input-referred noise spectral density values ($W_{gate}L_{gate}S_{VG}f$), computed from measured I_D noise spectral density, for HfO_2/[TiN/TiAl/TiN]/W *vs.* HfO_2/TiN/W RMG-HKL devices. Results are in line with the ITRS 1/f noise roadmap, slightly improved for [TiN/TiAl/TiN] stacks which have reduced EOT due to an Al-induced remote scavenging effect [6].

In FinFET-based devices, due to full depletion of the narrow fins (W_{Fin}≤15nm), V_T tuning options are limited to EWF engineering. And even if, when compared to planar bulk devices, FinFETs need smaller EWF shifts from mid-gap to reach low or high-V_T targets (Fig.8) [7], their 3D-nature poses challenges to obtain controlled EWF on all 3 channels (Fig.9). Fig.10 shows that low EWF values (≥4.25eV) are obtained with ALD-[TiN/TaSiAl/TiN] stacks, and EWF↓ with ↑TaSiAl thickness and ↓TiN thickness underneath. Thinner films are required to fit scaled gate trenches, and in this regard the low-EWF values (~4.3eV) obtained with ~2nm TaSiAl (with ~1.7nm TiN underneath) are particularly attractive. Al is detected mainly at the bottom of the TaSiAl layer and in the TiN underneath (Fig.11), with lower J_G measured, at similar EOT~9Å, *vs.* [TiN/TiAl/TiN] stacks (Fig.12). TEM images in Fig.13 confirm the AR-independent nature of TaSiAl. Implementation in planar flow yields well-behaved devices with ΔV_T *vs.* [TiN/TiAl/TiN] devices in agreement with EWF extracted from capacitors in Fig.10. An additional scheme pursued for n-EWF engineering that could be extendable to FinFETs and very narrow gates is illustrated in Fig.14: Al diffusion from Al fill-metal [5,8] into underneath TiN layer on HfO_2. Figs.15,16 show that with proper liner choice prior to Al-fill deposition, besides the requirement for suitable filling properties, good low-V_T control and healthy ITP characteristics can be obtained for high AR (PMOS) NMOS devices, corresponding to (no) Al diffusion into the underneath TiN layer. Compared to the lower-AR [TiN/TiAl/TiN] devices, they show similar permanent (P) and recoverable (R) BTI degradation components, indicative of similar interface states and traps in the stack (Fig.17) [9].

Conclusions

Tight low-V_T NMOS distributions for L_{gate}≥35nm planar devices achieved through controlled TiN/(RF-PVD TiAl)-alloying, using RF-PVD TiN for minimized gate resistance or ALD-TiN for reduced J_G. Potential solutions for very narrow gates and FinFETs include: controlled Al diffusion from Al fill-metal in high AR gate trenches, and conformal, lower-J_G ALD-TiN/TaSiAl. Overall, Al-rich TiN *vs.* TiN EWF-metals showed comparable BTI, slightly reduced EOT, improved noise and healthy DC characteristics.

References

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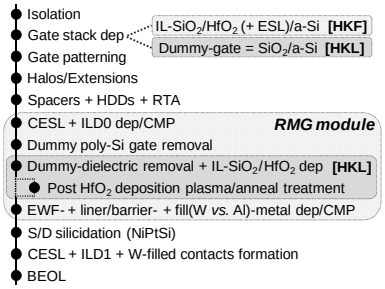

Fig.1 – Schematics of process flow used for fabrication of replacement high-k/metal gate (RMG) devices: with high-k first (HKF) or both high-k and metal deposited last (HKL). This work focus on RMG-HKL.

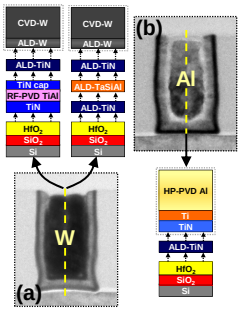

Fig.2 – Schematics of gate stacks (as-deposited) evaluated in this work for n-EWF engineering through: a) TiN/(RF-PVD TiAl and ALD-TaSiAl)-alloying; b) Al diffusion from fill-metal.

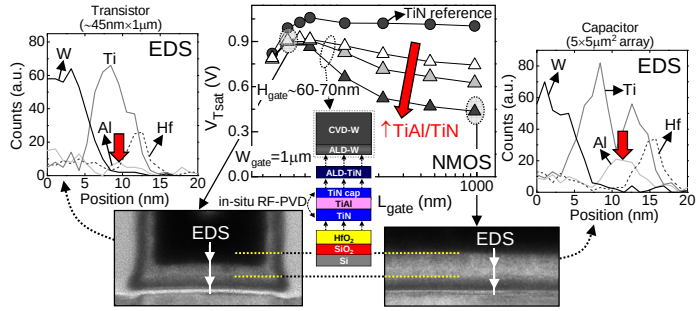

Fig.3 – TEM and EDS analysis show thicker RF-PVD [TiN/TiAl/TiN] stacks (⇒ higher Al content) in larger devices which have lower gate aspect-ratios (H_{gate}~60-70nm). This results in less Al-rich TiN on HfO_2 for scaled devices ⇔ less n-type EWF ⇒ V_T increase for smaller L_{gate} NMOS devices.

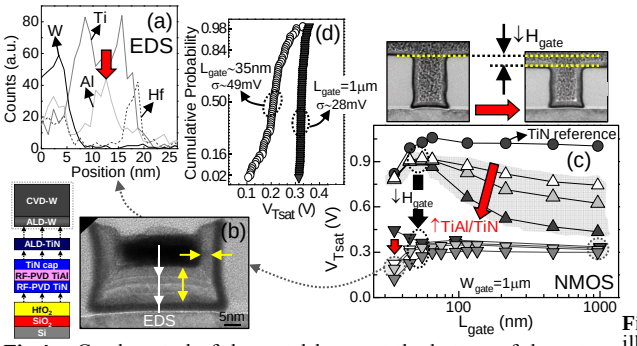

Fig.4 – Good control of the metal layers at the bottom of the gate trenches is achieved with RF-PVD TiAl/TiN thicknesses ratio optimization and H_{gate} reduction (= reduced gates AR), as shown by EDS and TEM: a) strong Al signal detected in small devices; b) good layers thicknesses control at center and gate edges, with minimal sidewall deposition. This leads to good $V_T(L_{gate})$ control (c,d).

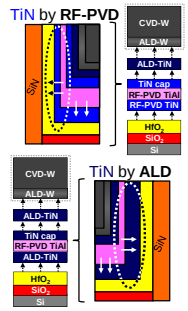

Fig.5 – Schematics to illustrate TiN deposition options in [TiN/TiAl/TiN] stacks: by RF-PVD (with minimal sidewall deposition) *vs.* by ALD (conformal).

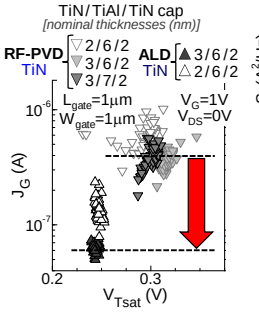

Fig.6 – Reduced J_G values with ALD-TiN due to improved sidewall coverage. It allows no preferential paths for Al diffusion, through TiN, into HfO_2 at gate sidewalls.

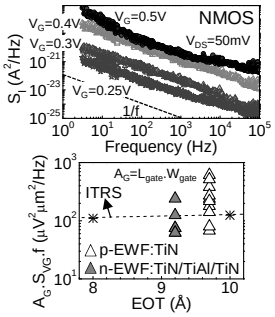

Fig.7 – On top, example of LF-noise spectra measured in linear operation at various V_G. Normalized S_{VG} values in line with ITRS 1/f noise roadmap, with slightly improved noise and reduced EOT for [TiN/TiAl/TiN]stacks (bottom).

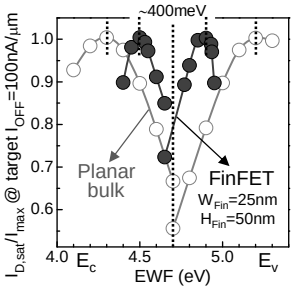

Fig.8 – Compared to planar bulk, FinFET-based devices require smaller EWF shifts for low-V_T applications, with optimum EWF calculated to be ±200meV shifted from mid-gap [7].

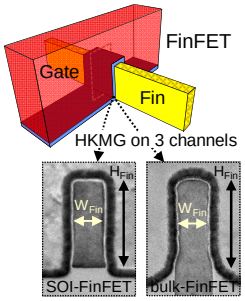

Fig.9 – Schematics (top) and TEM images (bottom) of FinFETs. A conformal high-k/metal gate process is required for good EOT - V_T (set by EWF-metal) control on the three channels.

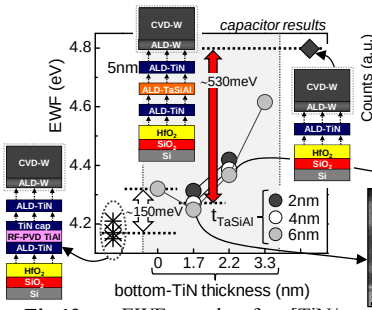

Fig.10 – EWF results for [TiN/TaSiAl/TiN] stacks deposited by ALD on HfO_2, with vacuum-breaks in-between layer depositions. EWF↓ with ↑TaSiAl thickness and ↓TiN thickness underneath. TaSiAl scaled down to ~2nm thickness with low EWF values (~4.3eV).

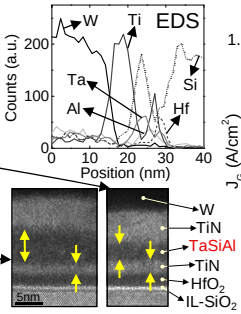

Fig.11 – EDS results show Al detected mainly at the bottom of TaSiAl and in the TiN layer underneath (figure on top), for varying TiN/TaSiAl thicknesses (TEM at the bottom).

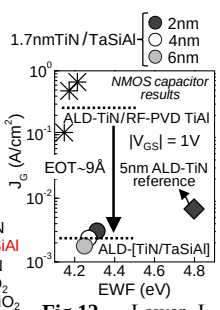

Fig.12 – Lower J_G values measured for ALD-[TiN/TaSiAl] *vs.* [TiN/TiAl/TiN] stacks, at similar EOT~9Å.

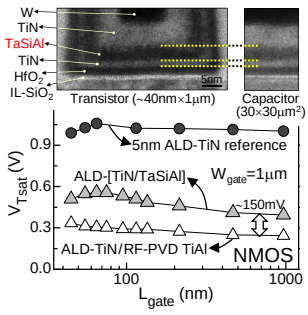

Fig.13 – TEM images show that similar ALD-[TiN/TaSiAl/TiN] stacks are obtained in ≠ gate AR devices (on top). ΔV_T *vs.* [TiN/TiAl/TiN] stacks in planar devices confirm ΔEWF results extracted in simple capacitors (at the bottom).

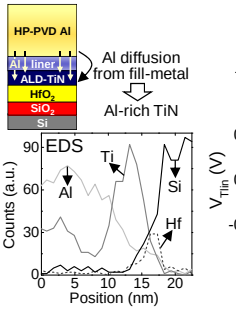

Fig.14 – EDS show diffusion of Ti from TiN/Ti-liner into the Al-fill, and of Al into the underneath TiN layer on HfO_2.

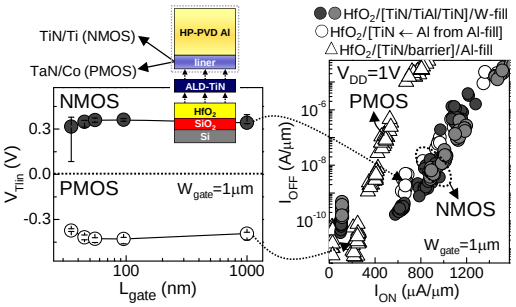

Fig.15 – Depending on the liner choice prior to Al-fill deposition, good low-V_T control can be obtained for PMOS (TaN/Co) and NMOS (TiN/Ti) with high AR gates.

Fig.16 – Healthy ITP characteristics for NMOS devices with n-EWF set by Al diffusion from the Al-fill into the underneath TiN layer on HfO_2.

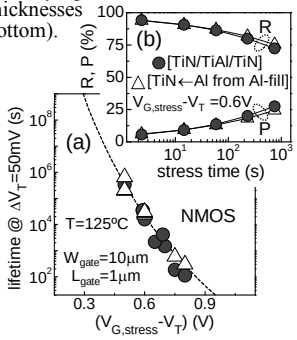

Fig.17 – Devices with n-EWF engineered through Al diffusion from fill-metal show overall BTI-lifetime (a), and R and P degradation components (b) comparable to those of [TiN/TiAl/TiN] devices.