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Enhanced Hole Mobility in High-k Gated pMOSFETs by Dislocation-free Epitaxial Si/Ge Super-lattice Channel

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1. Introduction

As the gate oxide thickness of MOS devices becomes thinner, the high-k gate dielectric has been implemented to replace SiO_2 or SiON for nano-scale MOS device applications. However, a reduction in channel mobility is also encountered. A promising technique to solve this issue is to alternate Si channel with high mobility material, like Ge, which can offer two times higher electron mobility and four times higher hole mobility than Si [1]. Besides, the mobility improvement of Ge MOS can be increased by compressive strain [2]. Nevertheless, the Ge and SiGe MOSFET have several concerns: the cost of pure Ge wafer is higher, the method of Ge grown on Si is complicated [3], Ge up-diffusion after high temperature annealing resulting in degradation of device performance [4], and the mobility improvement is not enough for SiGe channel with low Ge content. In this work, a dislocation-free epitaxial super-lattice (SL) channel with Si/Ge period stacks is proposed for MOS device to achieve a high mobility and also maintain a good quality of gate dielectric.

2. Experimental

MOSFETs with Si, $Si_{0.7}Ge_{0.3,}$ and Si/Ge super-lattice channel were fabricated on n-type Si (100) wafer, as shown in Fig. 1. A 2 nm thick HfO_2 were deposited by an atomic layer deposition (ALD). Then, a 50 nm thick TaN film was deposited by a sputtering to serve as the metal gate. For dopant activation, annealing treatments for Si, $Si_{70}Ge_{30,}$ and Si/Ge super-lattice channel were carried out at 950, 800, 650 ^{o}C, respectively, for 30 s in N_2.

3. Results and discussion

Fig. 2 shows the schematic cross-section of SL channel with repeating 11~20 periods of the Si 8 Å/Ge 4~8 Å stacks. Fig. 3 shows the HR-TEM images of the SL virtual structures with (a) Si 8 Å/Ge 4 Å and (b) Si 8 Å/Ge 8 Å stacks. Fig. 4 shows the HR-XRD rocking curve spectra of the SL structures, which reveal that the SL structures are epitaxially grown along Si (001) plane. The R_{rms} values from the 10 μm x 10 μm AFM scans of the 8/4 and 8/8 SL structures are 1.54 Å and 1.35 Å, respectively. Fig. 5 (a) shows the comparison of EOT and leakage current density for MOS devices with Si, SiGe, and SL channels after a PDA at 700 ^{o}C, indicating the Ge up-diffusion may be minor. Fig. 5 (b) shows the current versus bias voltage for S/D junctions in MOSFET with Si, SiGe, and SL channels, respectively, after various activation temperatures. Since the SL sample has lower S/D activation temperature (650 ^{o}C), it is more suitable to integrate high-k dielectric process. Fig. 6 shows (a) the C-V hysteresis and (b) Gm*EOT*L/W versus gate voltages of devices with Si, SiGe, and SL channels, indicating good interface quality with employing SL channel. Fig. 7 shows (a) Id–Vg and (b) Id–Vd characteristics of MOSFETs with Si, SiGe, and SL channel. Good MOSFET characteristics are observed for SL sample, such as a relatively high drive current, an acceptable subthreshold swing (*SS*) of 84 mV/dec, a lower I_{OFF} leakage of 5×10^{-12} A, and large on-off ratio (over 8 orders). It can be attributed to higher mobility, minor Ge up-diffusion, good S/D junction, and a compressive stress with fully-strain in Ge layer achieved by SL channel. Fig. 8 shows hole mobility as a function of the effective electric field for MOSFETs with Si, SiGe, and SL channel. The peak hole mobility of the device with SL channel is about 150 $cm^2/(V \cdot s)$, which is enhanced by about 100 % and 30 % as compared to that with Si and SiGe, respectively. Results in this work are benchmarked with some reported ones as listed in Table I. Compare to the SL sample, most other devices have larger EOT values; for those MOSFET devices with small EOT values and high Ge content, the mobilities are similar to the SL sample.

4. Conclusions

This work demonstrated a high-performance MOSFET with epitaxial SL on Si substrate. SL channel is characterized to have extremely low surface roughness, dislocation-free structure and fully-strained Ge layers. This design achieves good performance in terms of high mobility and on-off ratio. The temperature of S/D annealing at 650 ^{o}C is also promising to integrate with high-k/metal gate stack.

References

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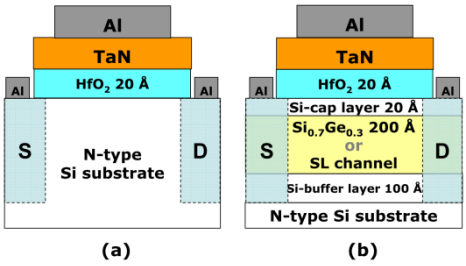

Fig. 1 The schematic cross-sections of pMOSFET devices with (a) Si and (b) SiGe or Si/Ge super-lattice (SL) channel.

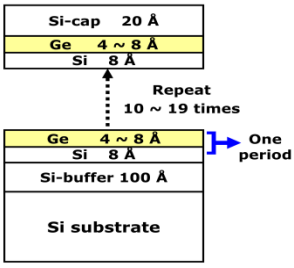

Fig. 2 The schematic cross-section of SL channel with different thicknesses of Ge layers.

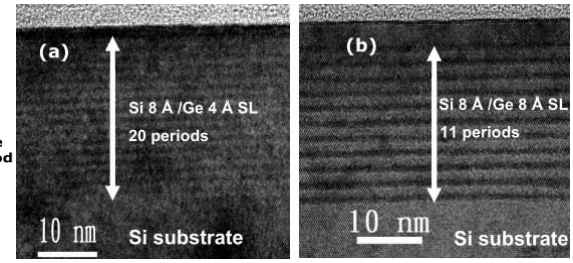

Fig. 3 The HR-TEM images for the as-deposited (a) 8/4 and (b) 8/8 SL structure. Clear interfaces between Si and Ge indicate good epitaxial structure of SL channel.

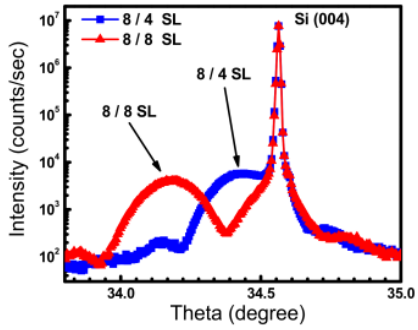

Fig. 4 The HR-XRD rocking curve spectra of 8/4 and 8/8 SL structures along Si (004) plane.

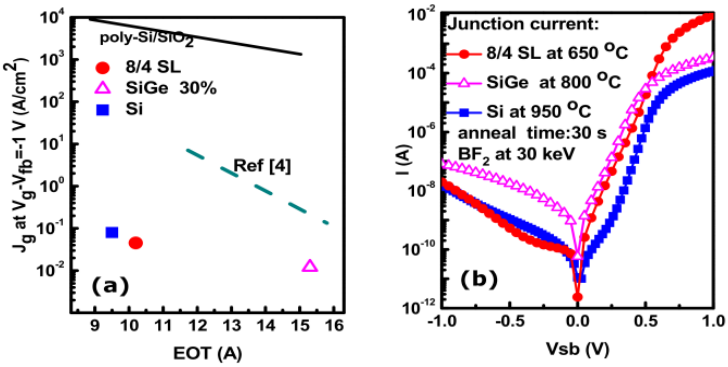

Fig. 5 (a) Comparison of leakage current density and EOT for MOS devices. (b) The current for S/D junction in MOSFET devices with Si, SiGe, and SL channel after various S/D activation temperatures.

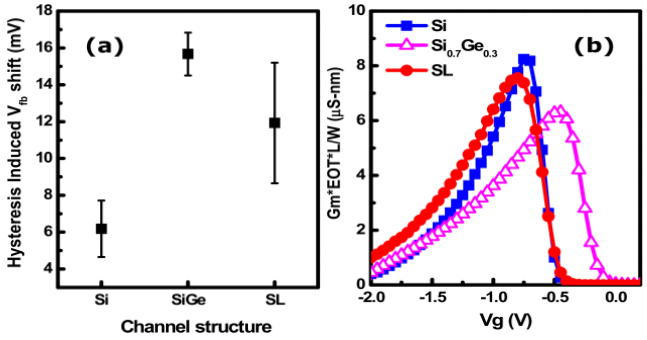

Fig. 6 (a) Capacitance-voltage hysteresis and (b) Gm*EOT*L/W versus gate voltage for devices with Si, SiGe, and SL channel.

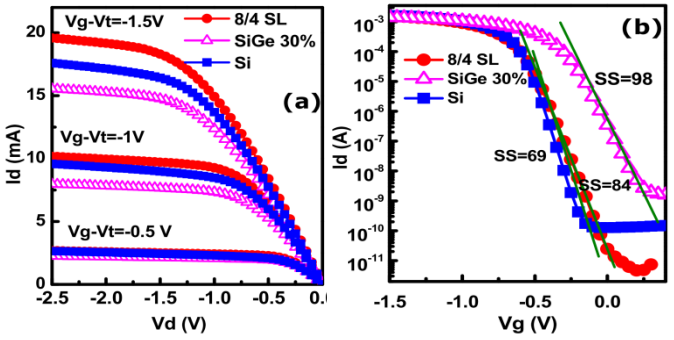

Fig. 7 (a) Id-Vg and (b) Id-Vd characteristics of MOSFETs with Si, SiGe, and SL channels, indicating good electrical characteristics of the device with SL channel.

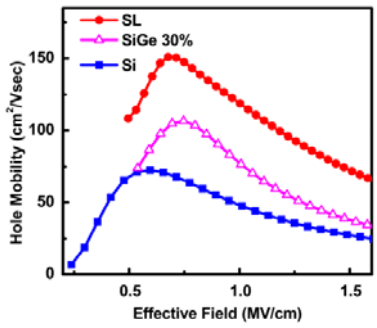

Fig. 8 Hole mobility as a function of the effective electric field for MOSFETs with Si, SiGe, and SL channel.

Table I Comparison of main electrical parameters about MOSFET with SiGe or Ge virtual channels

Channel structure	Max-μ_h ($cm^2 V^{-1} s^{-1}$)	High-k dielectric	EOT (Å)
8/4 SiGe Super-lattice [This work]	150	2nm HfO_2	10
Epitaxial pure Ge [5]	170	5 nm HfO_2	-
Epitaxial Pure Ge [6]	400	GeO_2+4.5 nm Al_2O_3	-
Solid phase epitaxy Ge [1]	350	SiO_2	>25
Epitaxial $Si_{0.25}Ge_{0.75}$ [7]	140	HfSiOx	10
Epitaxial $Si_{0.5}Ge_{0.5}$ [7]	180	HfSiOx (flash anneal)	10
Epitaxial $Si_{0.45}Ge_{0.55}$ [8]	140	-	8.5