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RMG Technology Integration in FinFET Devices

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Abstract

In this work, the advantages and integration challenges of RMG FinFET devices are presented. RMG integration in FinFET devices is successfully demonstrated with gate poly-Si CMP identified as a key process step for integration. It is also shown that RMG FinFET devices exhibit improved electrical characteristics with respect to Gate-First integration.

Introduction

As the downscaling race continues to improve the performance of integrated circuits, the traditional 'planar bulk transistor' architecture is facing serious physical problems and new architectures must be considered. Among these structures, Multiple-gate transistors such as FinFETs allow relaxing the tight scaling rules thanks to improved short-channel-effect (SCE) control [1]. Recently, FinFETs fabricated on bulk wafers gained momentum due to the possibility of keeping performance close to transistors built on SOI wafers, while having several key advantages over SOI such as low cost, low defect density, and a process flow similar to conventional bulk CMOS technology [2,3]. In 2012, Intel started to ship microprocessors using Bulk FinFET transistors for their 22nm node [4]. Moreover, Replacement Metal Gate (RMG) schemes are being considered in order to avoid early aggressive thermal budget for high-k/metal gate stacks [5]. RMG integration can be derived in two flavours: "high-k first" (HKF) where the high-k is deposited at beginning of process and protected by an Etch Stop Layer (ESL) during dummy gate removal or "high-k last" (HKL) where the high-k is deposited at end of process. In this work, we show for the first time advantages and integration challenges of RMG FinFETs using HKF or HKL schemes, and their comparison with Gate-First (GF) integration.

Device fabrication

The integration flow for bulk FinFET devices is illustrated in Fig. 1. Three different schemes are investigated and compared: GF in which the final high-k metal gate-stack is deposited right after well formation while for RMG, a dummy gate is instead used. The dummy gate is removed after source and drain (S/D) silicidation. In HKF, only the poly-Si gate is etched away, leaving ESL and HfO_2 underneath. Hence, the ESL protects the high-k during poly etch step. The sacrificial poly gate is then replaced by a Work Function Metal (WFM) and a W fill-metal. In HKL, the whole dummy gate stack, including poly-Si and oxide, are etched away, followed by an Interfacial Layer (IL)-oxide growth using oxidation in O_3, 1.8 nm HfO_2, WFM and W fill-metal depositions. TEMs (Fig. 1) show cross-section views of the gate in an HKL FinFET device, respectively perpendicular and along Fin. The RMG module used in this work is close to one applied on planar devices [6]. However, topography in active area introduced by Fins requires Chemical Mechanical Polishing (CMP) of the poly gate. This planarization reduces the gate step-height between active area and field oxide and thus eases photolithography and etch steps (Fig. 2). As shown in Fig. 3, dummy poly gate patterning is a critical step in bulk FinFET HKL integration. Gate etch is carried out through a 2-steps RIE: a Main Etch (ME) providing a good gate profile while showing poor oxide selectivity, followed by a Soft Landing (SL) step giving good selectivity towards oxide but a sloped gate profile. As a consequence, for a given gate poly thickness on Fins, too long ME consumes all gate oxide and results in Fins attack. On the other hand, long SL step results in tapered gate profile. As a consequence, for HKL dummy gate, a tradeoff exists between profile and pitting in Fins. Moreover, Fig. 3 indicates an optimum ME time at 17s for 100 +/- 10 nm poly showing no pitting in Fins while maintaining a good gate profile. Nevertheless, this restricts gate height range to 90-110 nm on Fins after poly CMP. Another advantage of planarization step at dummy gate level is an increase in ILD0 thickness on active area. The ILD0 stack consists in nitride Contact Etch Stop Layer (CESL) and oxide. As illustrated in Fig. 4, for different ILD0 over-polishing time, planarization of dummy gates always increases ILD0 oxide margin on Fins compared to non-polished gates.

Electrical results

Fig. 5 shows the benefit of gate-last process in terms of device performance. RMG FinFET PMOS show 25% higher I_{ON} than GF devices at 10^{-7} A/µm I_{OFF}. Little difference is observed between HKF and HKL. Additionally, RMG devices exhibit significantly lower threshold voltage V_T values compared to GF as shown in Fig. 6. V_T roll-off (Fig. 6) and DIBL (Fig. 7) are maintained for both RMG HKF and HKL FinFET PMOS. For a same gate stack: 1.8 nm HfO_2 / 5 nm ALD-TiN, HKL FinFET PMOS devices show 250 mV long channels V_T shift with respect to GF (Fig. 8). As a consequence, V_T difference between GF and HKL can be attributed to thermal budget impact on gate stack. Moreover, both GF and HKF devices exhibit same dependency towards ALD-TiN thickness. With respect to GF, V_T of HKF FinFET PMOS devices is further decreased by depositing 5 nm ALD-TiN WFM during RMG module. From Fig. 8, it also appears possible to control V_T of RMG devices by carefully tuning the TiN thickness. Another advantage of HKL approach is illustrated in Fig. 9: for different Fin widths, HKL FinFET PMOS devices display smaller Capacitance Equivalent Thickness (CET) compared to HKF and GF, but with a very comparable gate leakage. This is likely due to the fact that in HKL devices the high-k only sees a limited part of integration thermal budget whereas in HKF and GF schemes the gate stack has to withstand the whole thermal budget. This includes high temperature junction anneals, which can degrade high-k layer. On the NMOS side, the threshold voltage of long channels RMG FinFETs is reduced by introducing TiAl between TiN layers in gate stack (Fig. 10). Indeed, Al is known to diffuse towards high-k, which shifts gate stack effective work function towards n-type. V_T is further decreased by increasing TiAl thickness thus increasing the Al diffusion source. However, roll-off is not maintained at short gate lengths because of poor step-coverage of PVD TiAl on fin sidewalls. Other deposition techniques such as ALD could be necessary to ensure good conformality.

Conclusion

In this paper, we demonstrated the integration of RMG in FinFET devices and identified gate poly-Si CMP as a key process step for this integration. Furthermore, RMG FinFET devices show improved electrical characteristics compared to GF. V_T tuning for both N and PMOS through WFM in RMG FinFETs is also shown.

References

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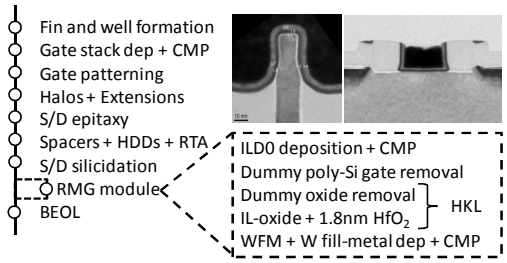

Fig. 1: Process flow for Gate-First (GF) and gate-last (RMG) high-k first (HKF) / high-k last (HKL) FinFET devices.

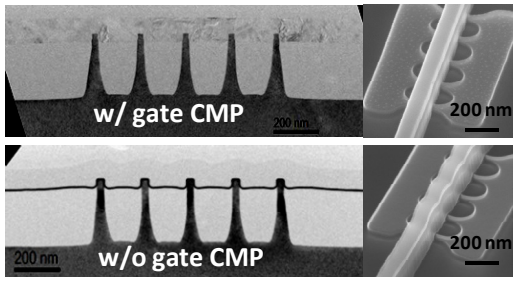

Fig. 2: TEMs and SEMs of gate with and without CMP. Planarization reduces gate step-height between active area and field oxide and eases photolithography and etch steps.

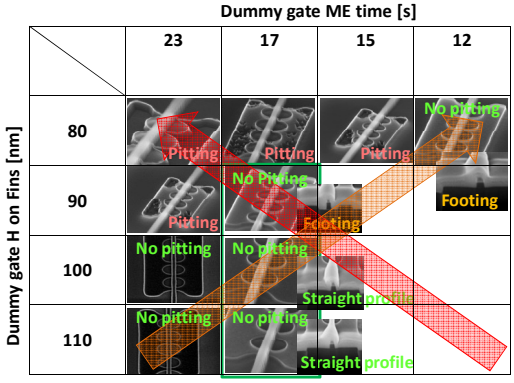

Fig. 3: HKL dummy gate patterning illustrating the necessary trade-off between gate profile and fin pitting.

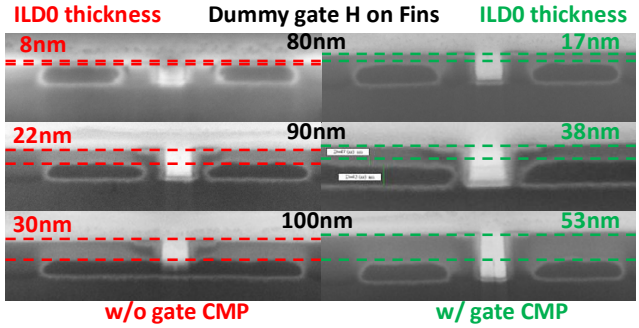

Fig. 4: Impact of poly gate CMP on ILD0. For different ILD0 over-polishing time, planarization of dummy gates always increases ILD0 oxide margin on fins compared to non-polished gates.

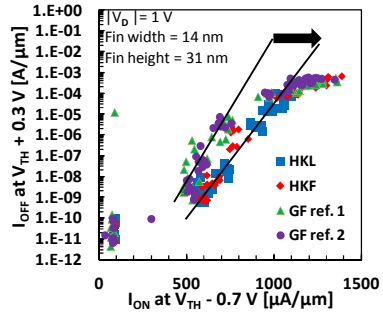

Fig. 5: I_{ON}-I_{OFF} for GF and RMG HKF/HKL bulk FinFET PMOS devices at $|V_D|$ = 1 V, (V_G -V_T) = -0.7 V (ON-state) and (V_G -V_T) = 0.3 V (OFF-state).

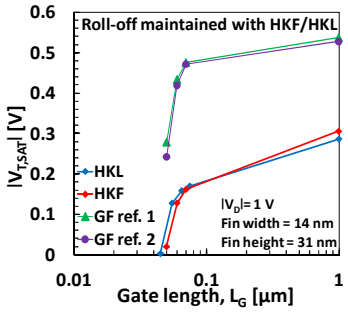

Fig. 6: $V_{T,SAT}$-L_G for GF and RMG HKF/HKL bulk FinFET PMOS devices showing that V_T roll-off is maintained for both RMG HKF and HKL.

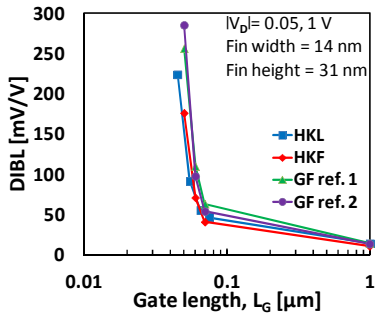

Fig. 7: DIBL for GF and RMG HKF/HKL bulk FinFET PMOS devices showing no short channel gate control degradation due to the RMG integration.

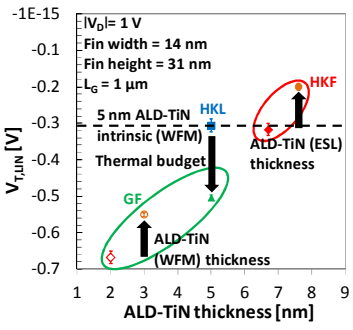

Fig. 8: $V_{T,LIN}$ of GF and RMG HKF/HKL bulk FinFET long channel PMOS devices showing possibility to control threshold voltage with ALD-TiN thickness.

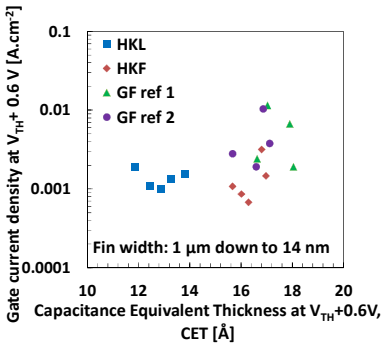

Fig. 9: Gate Leakage versus Capacitance Equivalent Thickness (CET) at V_{TH} + 0.6V for TiN/HfO2 gate stack in gate-first and RMG HKF/HKL bulk FinFET PMOS devices.

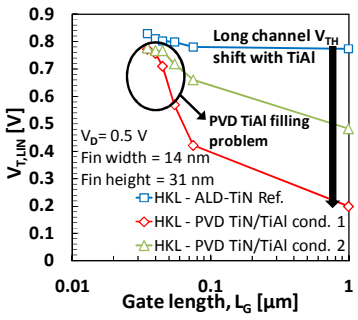

Fig. 10: $V_{T,LIN}$-L_G for gate-first and RMG HKL bulk FinFET NMOS devices with 2.5 nm TiN/5 nm TiAl50%/2 nm TiN (cond.1) and 2.5 nm TiN + 3 nm TiAl50%/2 nm TiN (cond.2).