

Fabrication and Demonstration of Ultra Short Channel Atomically Thin SOI MOSFETs (AT-FET) Using Anisotropic Wet Etching and Lateral Dopant Diffusion

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1. Introduction

Studies of sub-10 nm MOSFETs are significant for the embodiment of ultra-low power devices at 15 nm technology nodes and beyond. They have been reported using bulk MOSFET [1-3], FinFET [4], ultra thin SOI [5], and nanowires [6-9] in combination with advanced engineering of junctions and reduction of parasitic resistance. Control of channel thickness is also a critical issue [10-12]. We present in this work ultra short channel Atomically Thin SOI MOSFETs (AT-FET) fabricated using simple techniques. The atomically thin channel structures were prepared by V-groove formation using anisotropic wet etching. Lateral dopant diffusion was promoted to reduce parasitic resistance and to operate AT-FETs in a junctionless-FET manner [13]. Performances of nanometer MOSFETs are demonstrated.

2. Experimental

Process flow of AT-FETs is shown in Fig. 1. Surface orientation of SOI is (100), and the channel directions of FETs are $\langle 110 \rangle$. Using the oxide masks that were patterned by *e*-beam lithography, V-grooves were formed by anisotropic wet etching using Tetramethylammonium hydroxide (TMAH) solution. HfO_2 dielectric film and poly-Si electrode film were deposited by ALD and CVD. Gate patterns with 140 nm-length were prepared on V-grooves using *e*-beam lithography and reactive ion etching. Following to the BF_2^+ ion implantation (15 kV , $1 \times 10^{15} / \text{cm}^2$), activation anneal was processed at 1000°C for 10 min. The long period annealing promotes lateral dopant diffusion under V-grooves and reduces parasitic resistance. Devices were finished by metallization and forming gas anneal in H_2 gas at 400°C .

3. Results and Discussion

Cross sectional TEM image of an AT-FET is shown in Fig. 2. The V-groove consists of Si (111) facets, and the apex is approaching to the interface of BOX. The thickness of SOI in source and drain regions is 80 nm. It contributes to the reduction of parasitic resistance without selective epitaxial growth technique.

Magnified TEM images of three AT-FETs are compared in Fig. 3. They were prepared with different sizes of oxide openings (L_V in Fig. 1). The channel thicknesses (T_{CH}) achieved are 6.2 nm, 3.1 nm, and less than 1 nm, respectively. The channel lengths (L_{CH}) are 3 nm and irrespective of the channel thickness. In this experiment, unintentional oxidation of Si interfaces both at top and bottom of HfO_2 film was serious, and the total dielectric thickness increased to 10 nm. The apex of the V-groove is rounded by the excess oxidation, and it determined the channel length. Thus further scaling of channel length is

possible by the suppression of interfacial SiO_2 growth.

Transfer characteristics of AT-FETs corresponding to Fig. 3 are shown in Fig. 4. A large flow of drain currents suggests that parasitic resistance is reduced effectively by the lateral dopant diffusion into channel region. In case of the 6.2 nm-thick channel, the drain current is hard to control because the channel thickness is much larger than the channel length. It is improved by scaling the channel thickness to 3.1 nm and less than 1 nm, where 6 orders and 8 orders of magnitude drain current modulations are attained. The ON-currents are almost proportional to the channel thickness. Gate leakage currents are negligibly small for all cases. The “normally-on” behavior of these AT-FETs is caused by the large equivalent oxide thickness (about 7 nm) and the use of p^+ -type poly-Si gate in p-type junctionless-FET. EOT scaling and appropriate metal electrodes are effective to adjust the threshold voltages.

I_D - V_G curves of AT-FETs that were fabricated by the same L_V size on a wafer are plotted in Fig. 5. Performances of AT-FETs change largely in spite of the identical design and process. In the I_{ON} - I_{OFF} plots shown in Fig. 6, it is found that the changes of performances are aligned on a trend. We consider that the large changes of performances are caused by the accumulation of variations in lithography, wet etching, and oxidation processes. As the performances in Fig. 4 show, a change of 1 nm in channel thickness results in a drastic change in electrical performance. Thus atomic-scale precision is indispensable for the fabrication of future nanometer MOSFETs.

4. Conclusions

AT-FET is demonstrated as a simple way to fabricate nanometer MOSFETs. Excellent performances are obtained when the balance between the channel length and the thickness are maintained. AT-FET has a potential to control the device structures with atomic-scale precision. It will be a powerful means for the development of ultra-low power devices such as tunnel-FETs in which application of quantum effects becomes important.

Acknowledgements

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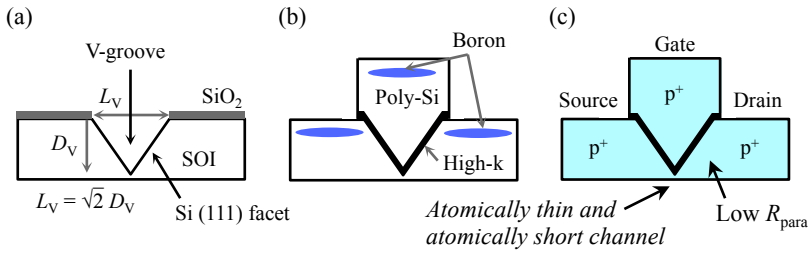


Fig. 1 Process flow of Atomically Thin SOI MOSFETs (AT-FETs). (a) V-groove formation by anisotropic wet etching using. (b) Gate stack formation and ion implantation. (c) Activation anneal (1000°C, 10 min).

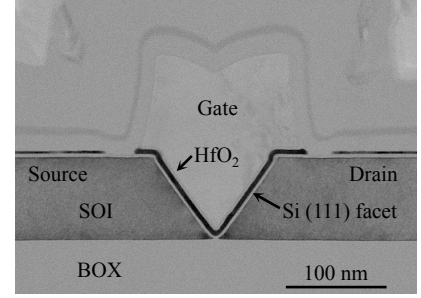


Fig. 2 Cross-sectional TEM image of Atomically Thin SOI MOSFET (AT-FET).

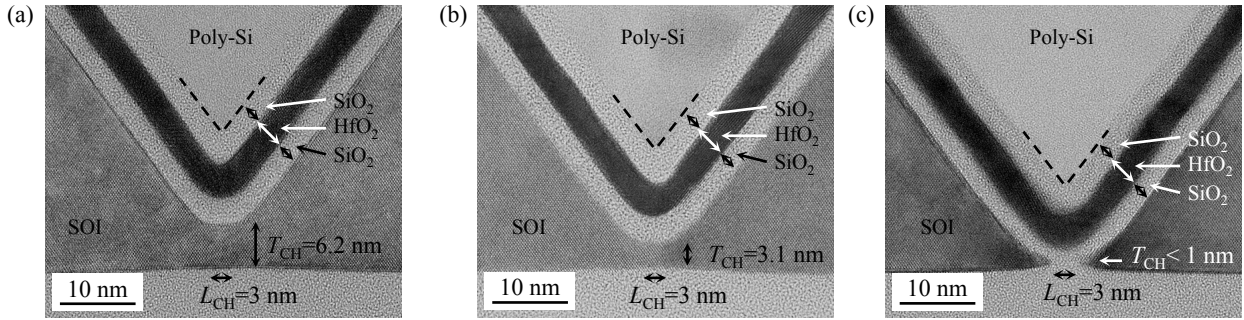


Fig. 3 Magnified TEM images of channel regions of AT-FETs on a single SOI wafer. The channel thickness T_{CH} and the channel length L_{CH} are (a) 6.2 nm and 3 nm, (b) 3.1 nm and 3 nm, and (c) less than 1 nm and 3 nm, respectively. Total thickness of the dielectric layer increased to 10 nm (SiO₂/HfO₂/SiO₂) by the oxidation of Si interfaces during the activation annealing.

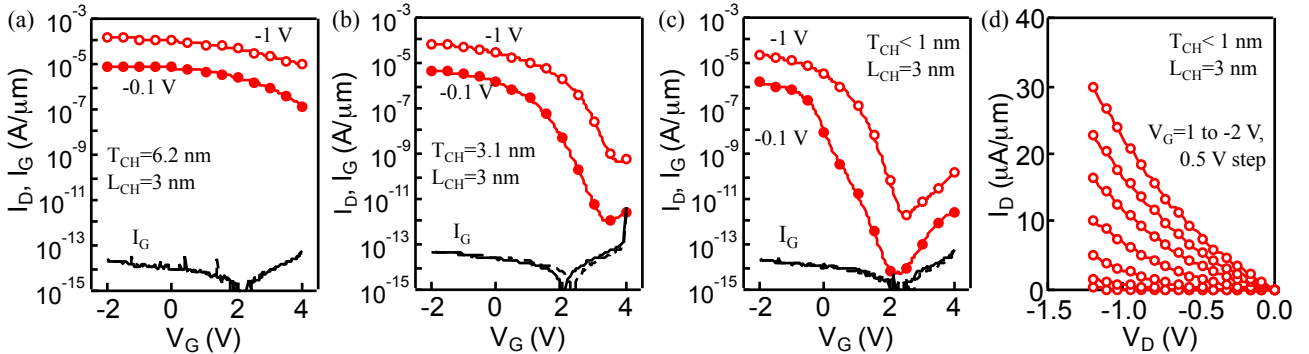


Fig. 4 I_D - V_G characteristics ($V_D = -0.1$ and -1 V) of AT-FETs ($L_{CH} = 3$ nm) corresponding to Fig. 3, (a) $T_{CH} = 6.2$ nm, (b) $T_{CH} = 3.1$ nm, and (c) $T_{CH} < 1$ nm, respectively. (d) I_D - V_D characteristics of AT-FET corresponding to Fig. 3(c), $T_{CH} < 1$ nm and $L_{CH} = 3$ nm. EOT of these devices is about 7 nm.

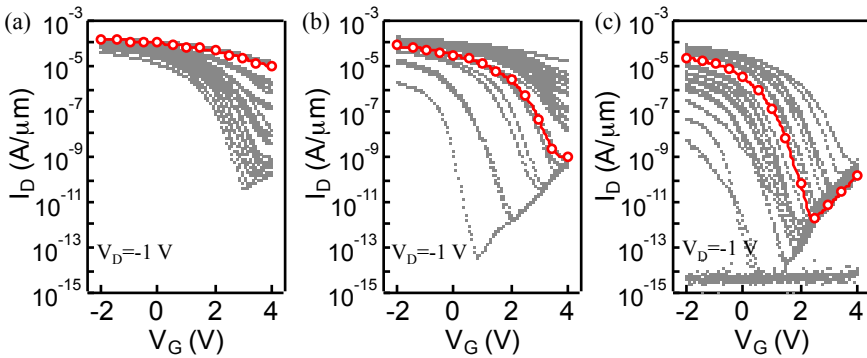


Fig. 5 I_D - V_G characteristics ($V_D = -1$ V) of 28 AT-FETs on a wafer that were designed with the same opening sizes (a) $L_V = 102$ nm, (b) 104 nm, and (c) 106 nm, respectively. Data of Figs. 3 and 4 are plotted with circles. Nanometer-scale variations in lithography, etching, and oxidation processes between devices on a wafer induced enormous difference in electrical performance.

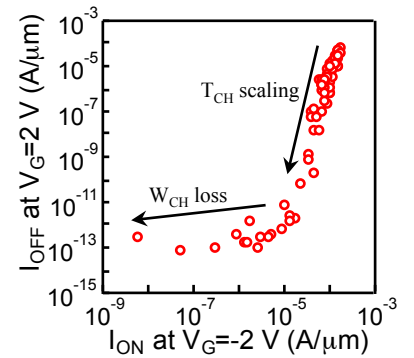


Fig. 6 I_{ON} - I_{OFF} plots of 84 AT-FETs in Fig. 5. I_{OFF} decreases with the scaling of channel thickness. The largest on/off ratio is obtained at atomically thin SOI FETs. Excess channel thickness scaling reduces I_{ON} which is caused by the loss of channel width (W_{CH}).