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Basic issues on alternative channel materials for Post-Si logic devices: from high mobility semiconductors to two dimensional atomic layers

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1. Introduction

New emerging research materials in the technology generation are currently laying the foundation for a post-Si era of complementary metal-oxide-semiconductor (C-MOS) devices [1]. Among them, alternative semiconductors with higher carrier mobility (high-μ) such as III-V compounds and Ge are taken into account as active channels along with non-conventional device architecture and concepts [2,3]. Not only the More Moore approach according to which "smaller is better" will be the unique guideline for engineering new device features [4], but also limiting power consumption is going to pose severe constraints for materials selection [5]. From a purely device scaling approach, a key-criterion is to preserve the drive current:

$$I_{D,sat} \propto \mu C_{ox}\left(V_g - V_t\right)^2 \qquad \text{Eq. (1)}$$

(where $I_{D,sat}$ is the drive current at saturation, V_g the gate bias, C_{ox}, the gate oxide capacitance and V_t the threshold voltage) against miniaturization by making use of proper technology boosters. In this respect, Ge and $In_{0.53}Ga_{0.47}As$ emerge as good mobility boosters respectively for n-type and p-type channels, thus proving as building blocks for a dual logic CMOS structure if co-integrated in a common platform and adequately coupled with high permittivity gate oxides (high-κ). The high-μ option adds to the booming interest in two dimensional (2D) layered materials with outstanding electronic properties such as graphene and graphene-like materials which may lead to new device functionalities or to new revolutionary issues of device physics [6]. In this respect, single layer MoS_2 field effect transistors (FET) has been recently demonstrated [7] and compelling evidences of the silicene, i.e. the graphene counterpart of Si, might overcome intrinsic limitation of graphene as active channel for logic applications [8].

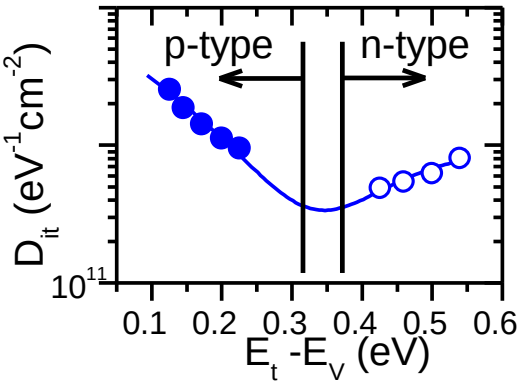
On the other hand, energy saving requirements are concerned with the optimization of the subthreshold swing of the device characteristics (SS) down to below the thermodynamic limit of 60 mV/decade, in other words:

$$SS = \frac{\partial V_g}{\partial(\log I_D)} \cong \left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) \ln 10 \frac{kT}{q} \cong 60 \text{ mV/dec} \qquad \text{Eq. (2)}$$

where C_d and C_{it} are the depletion and interface traps capacitance, kT/q is the thermal voltage. For sure an intrinsically lower range of operative bias as results in low band-gap Ge and $In_{0.53}Ga_{0.47}As$ can be helpful to downscale the dissipated power, however undesired electrical losses arising from the oxide-semiconductor interface or from parasitic capacitance/resistance can have a detrimental effect in the energetic balance of the device and must be minimized.

In particular, from Eqs. (1) and (2), either μ, V_t, and C_{it} can be severely affected by the electrical quality of the interface. Therefore interface optimization, i.e. minimization of the interface traps, is one of the mandatory tasks for high-μ based MOS capacitors to address both scaling and energy saving requirements. This effort can be tackled in high-μ semiconductors by selecting proper passivation treatments and unraveling the inherent basic physics. In the present review work, the density of interface traps throughout the semiconductor energy gap (D_{it} distribution) is taken as a reference property for discussing the general features of the interfaces of Ge and $In_{0.53}Ga_{0.47}As$ substrates with high-κ thin films or passivation layers.

Finally consideration will be open to graphene-like semiconductors, namely the silicene, as candidates for the ultimate scaling of device features.



.**Fig. 1** Typical D_{it} distribution of GeO_2/Ge based MOS capacitors (both p-type and n-type).

2. Ge-based interfaces

As GeO_2 is usually regarded as a good passivation layer material and a mobility booster for Ge-based MOSFETs [9], the Ge/GeO_2 interface has been referred to as a paradigmatic system to study the D_{it} distribution (shown in Fig. 1) as a function of the process parameters and in relation with

other passivation layers.

In particular, the electrical analysis of the Ge-based MOS capacitors has been tentatively correlated with more specific investigations of the electronic interfacial properties, including electrically detected magnetic resonance (EDMR) spectroscopy of paramagnetic traps or measurement of trap induced distortion of the interface energy band structure. Related findings are inherently concerned with basic Ge interface physics and might be of relevance for any kind of Ge stack implementation, e.g. not only in logics but also in Ge-based optoelectronics and photovoltaics for instances. Indeed, from EDMR the microstructure of the Ge dangling bond has been unambiguously identified and studied as a function of the oxidation process and of the surface orientation [10,11]. On the other hand, the high D_{it} in proximity of the valence band maximum which emerges as a common feature of Ge-based interfaces [12] has been shown to yield interface charge accumulation therein severely impacting the interfacial electronic band line-up.

3. $In_{0.53}Ga_{0.47}As$-based interfaces

With a similar scope to that used for Ge-based interfaces, the D_{it} distribution in Fig. 2 has been extracted from state-of-the-art $In_{0.53}Ga_{0.47}As$-based MOS capacitors incorporating an Al_2O_3 gate dielectric grown by trimethylalauminum-based atomic layer deposition (ALD). As main features of the D_{it} of $In_{0.53}Ga_{0.47}As$-based interfaces, a low D_{it} can be observed close to the conduction band minimum, whereas an increasing D_{it} results in the midgap region. The latter effect is mitigated by the "clean-up" effect of trimethylaluminum (TMA) initial pulses in the ALD process [13,14]; nonetheless several concerns on the nature of midgap traps and on the concomitant frequency dispersion in the accumulation regime in the capacitance-voltage curves still remain open and will be explicitly discussed. When approaching the valence band, Fermi level pinning is experienced from the low temperature electrical response of p-type $In_{0.53}Ga_{0.47}As$ MOS capacitor which is independently reflected by probing the local density of states around the Fermi level in $In_{0.53}Ga_{0.47}As$ surfaces. Upon benchmarking on the $Al_2O_3/In_{0.53}Ga_{0.47}As$-based MOS capacitors and taking benefit from the TMA-related interface chemistry, a TMA-based approach to the ALD of high-k oxide is here proposed in the attempt to address equivalent oxide scaling of $In_{0.53}Ga_{0.47}As$ -based MOS capacitors [15].

4. What's next?

A number of emerging research materials (e.g. nanowire, carbon nanotubes, 2D nanosheets, molecular transistors, negative capacitance dielectrics, etc.) can concur in re-defining the future backbone of Post-Si digital devices. In the present context, we limit our consideration to the recently discovered rise of silicene [16] as a graphene-like material option which aims at overcoming the unsuitability of graphene as active stack for FET devices and paving the way for a Si revival in nanoelectronics. The growth of silicene is here briefly introduced and future perspectives in logic applications will be discussed.

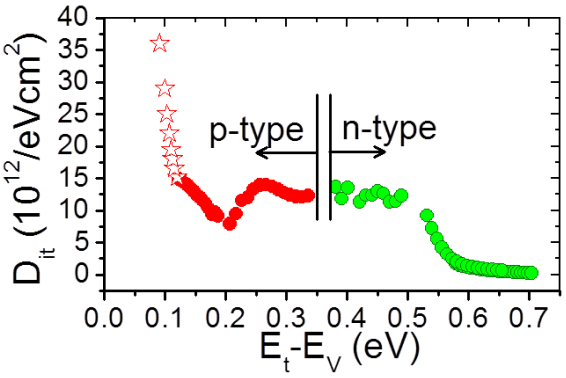


Fig. 2 Typical D_{it} distribution of Al_2O_3/ $In_{0.53}Ga_{0.47}As$ based MOS capacitors.

Acknowledgements

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