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High Mobility Poly-GeSn Layer Formed by Low Temperature Solid Phase Crystallization

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1. Introduction

A poly-Ge layer has attracted much attention for thin-film transistors (TFTs) with high mobility to realize system-in-displays [1], for photo sensors using TFTs and so on. On the other hand, in order to fabricate the TFTs on a glass or plastic substrate, low process temperature is required. Sn-Ge system is a typical eutectic alloy with eutectic temperature of 231°C. Therefore, introduction of Sn to the Ge grain might leads to low temperature crystallization. However, studies concerning a poly-GeSn formation have been hardly reported.

In this study, we have formed poly-GeSn layers at various temperatures by solid phase crystallization, and have investigated crystallization temperature, annealing temperature dependence of mobility and carrier concentration. Comparing these properties between poly-Ge and poly-GeSn layers, we found that the Sn incorporation is effective to decrease the crystallization temperature and to improve the mobility at low annealing temperature.

2. Experimental Procedure

The process flow of Ge and GeSn layers and the resulting sample structure are shown in Fig. 1(a) and 1(b), respectively. After cleaning Si wafers, a 1-μm-thick SiO_2 layer was formed by wet oxidation at 1000°C. 300-nm-thick Ge or GeSn layers with different Sn content were deposited by MBE at room temperature. The samples were annealed at various temperatures (T_a) for various times (t_a) in N_2 ambient. Crystallinity and electrical properties of the formed layers are evaluated by Raman scattering spectroscopy, XRD and Hall measurement.

3. Results and Discussion

Crystallinity of the Ge and GeSn layers at various annealing temperatures was confirmed by Raman scattering spectroscopy (Fig. 2). Crystallization occurred at 450°C for 5 hr for the Ge layer, while the GeSn layer with the Sn content of 2% was crystallized at 430°C for 5 hr. The low temperature crystallization was also observed in the sample with the Sn content of 0.2% (Fig.3). These results strongly suggest that the Sn incorporation is effective to reduce the crystallization temperature. In order to confirm grain growth, grain size for the Ge layer (Fig. 4(a)) and GeSn layers with the Sn content of 0.2 %(Fig. 4(b)) and 2% (Fig. 4 (c)) were observed by Raman mapping. In the Ge layer, the grains with size of ~1μm are distributed. Here, the observed grain is not a single crystal grain because the resolution of Raman mapping is around 1μm. Although the resolution is not enough, the differences of the grain growth can be observed by the Raman mapping. The grain enlarges up to ~3μm due to the Sn incorporation of 0.2%. In Sn content of 2%, no grain is observed, suggesting that the poly-GeSn layer is uniformly crystalized. On the other hand, the Sn content evaluated from the Raman peaks depends on T_a and t_a (Fig. 5). At 500°C and 10hr, almost all Sn comes out from the crystal grain. In contrast, at 430°C, the Sn content hardly changes after 10hr annealing. These results suggest that low temperature annealing or short t_a annealing at high temperature is needed for keeping the Sn content. In order to evaluate the crystal grain size, the Ge and GeSn layers were evaluated by XRD measurement. Figure 6 shows XRD spectra for the Ge and GeSn layers annealed at 450°C for 5hr. The sharp diffraction peaks for the GeSn layer were clearly observed compared with that for the Ge layer. Also, the full width half maximum (FWHM) for Ge(111) and GeSn (111) diffraction peaks were compared at various T_a (Fig. 7). We found that the FWHM values for the GeSn layer is smaller than that for the Ge layer, suggesting that the GeSn layer has large grains or high crystallinity compared with the Ge layer.

It is known that coexistence of poly-Ge and amorphous Ge grains in a layer induce high resistivity, because the amorphous Ge grain has a quite high resistivity[2]. Therefore, uniformity of the poly-Ge or poly-GeSn layer can be evaluated from resistivity measurement. The resistivity of the Ge layer annealed at temperature lower than 430°C is quite high, while the resistivity drastically decreases at 450°C (Fig. 8). Although the similar trend was observed in the case of the GeSn layer, the temperature decreasing the resistivity is lower than that for the Ge layer. Figure 9 shows annealing time dependence of the resistivity for the Ge and GeSn layers. We found that the time decreasing the resistivity of the GeSn layer is shorter than that for the Ge layer. These results mean that the Sn incorporation is effective to reduce the crystallization temperature. Also, this result is consistent with the results obtained by Raman analysis.

Also, the resistivity depends on carrier mobility and carrier concentration. Therefore, carrier mobility and carrier concentration in the poly-Ge and GeSn layers were evaluated by Hall measurement. In all samples, the carrier type was hole as well as a result reported in Ref. 3. As shown in Fig. 10(a), carrier concentration in the Ge layer slightly decreases with increasing T_a. On the other hand, in the case of the GeSn layer (Fig. 10(b)), T_a dependence is quite complicated. The carrier concentration annealed at 450°C is the smallest ($7\times10^{17}cm^{-3}$), which is attributable to the high quality cystallinity at the low temperature as shown in Fig. 7. Figures 11 (a) and (b) show T_a dependences of the mobilities for the Ge and GeSn layers, respectively. The mobility for the poly-Ge layer increases with increasing T_a, owing to the grain growth as shown in Figs. 2 and 7. Although origins of the complicated dependence for the carrier concentration and the mobilites have not clarified yet, possible reasons of the complicated behavior are the Sn evacuation from the crystal grain as shown in Fig. 5 and carrier depletion in the crystal grain[4]. However, it should be noted that the mobility of the GeSn layer annealed at 450°C for 5hr is 5 times larger than that for the Ge layer. These results indicate that the Sn incorporation leads to the low temperature crystallization, and that the Sn incorporation effectively improves the mobility.

4. Conclusions

Comparative study between the poly-Ge and the poly-GeSn layers reveals that the Sn incorporation is effective to decrease the crystallization temperature. Also, from the comparative study, we found that the Sn incorporation drastically improves the mobility in the GeSn layer annealed at low temperature.

References

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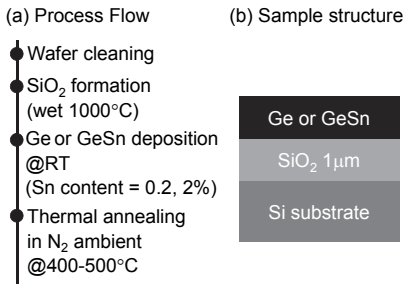

Fig. 1 (a) Fabrication process flow of the sample and (b) the sample structures.

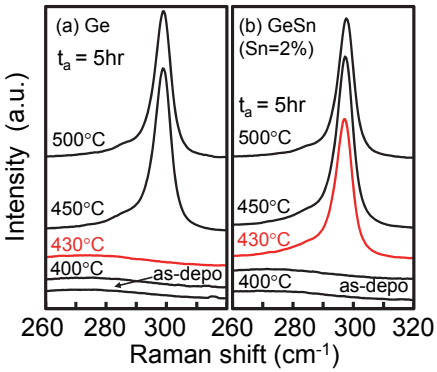

Fig. 2: Temperature dependences of Raman spectra for (a) Ge layer and (b) GeSn layer with Sn content of 2%.

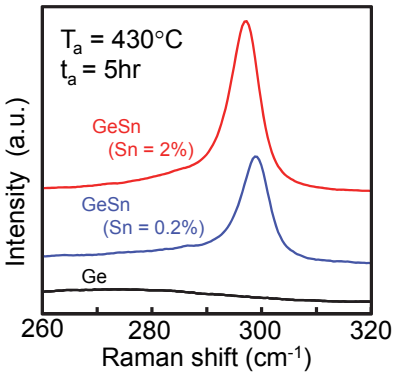

Fig. 3: Raman spectra for the samples with various Sn content.

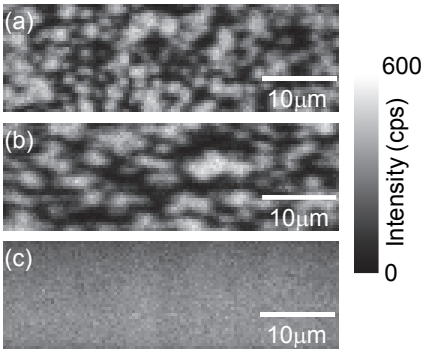

Fig. 4: Raman mapping of the samples for (a) Ge , (b) GeSn(0.2%), (c) GeSn (2%) annealed at 430°C for 5hr.

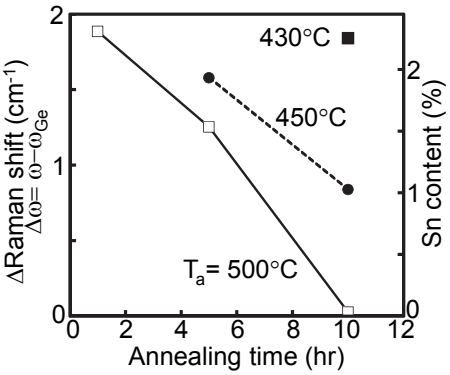

Fig. 5: Raman peak shifts based on Ge Raman peak as a function of annealing time. Here, initial Sn content N_{sn} is 2%.

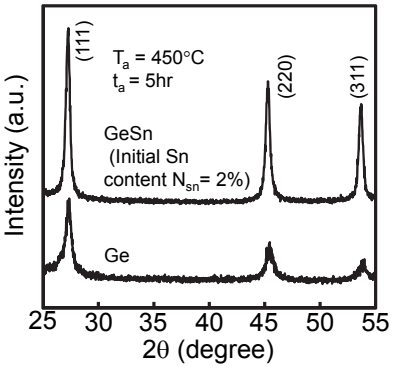

Fig. 6: XRD spectra for the Ge and GeSn layers annealed at 450°C for 5hr.

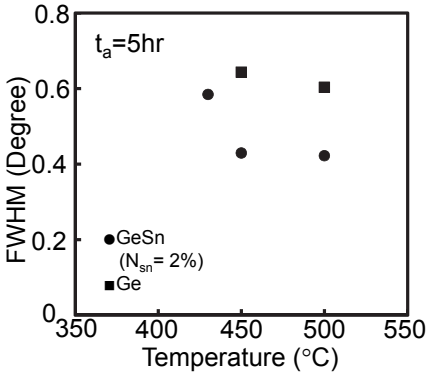

Fig. 7: Temperature dependence of full width half maximum of Ge (111) and GeSn (111) peaks measured by XRD.

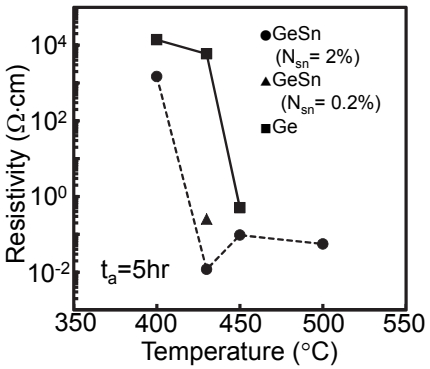

Fig. 8: Temperature dependence of resistivity for Ge, GeSn layer. Here, the annealing time t_a is 5hr.

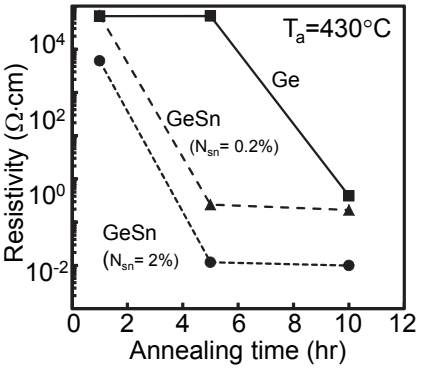

Fig. 9: Annealing time dependence of resistivity for Ge, GeSn layer annealed at 430°C.

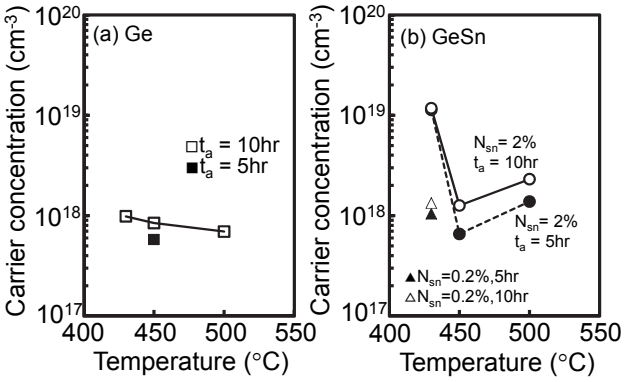

Fig. 10: Temperature dependences of carrier concentrations for (a) Ge, and (b) GeSn layer.

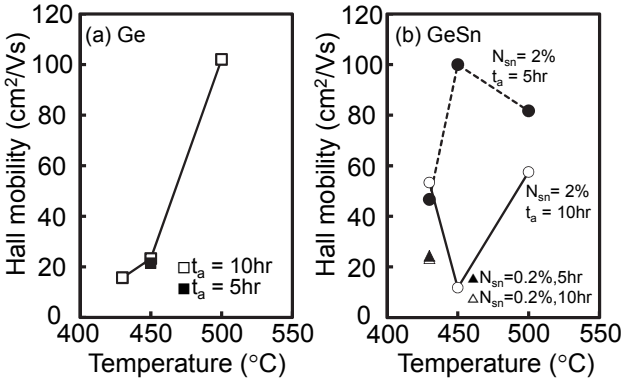

Fig. 11: Temperature dependences of Hall mobilities for (a) Ge, and (b) GeSn layer.