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W *vs.* Co-Al as Gate Fill-Metal for Aggressively Scaled Replacement High-k/Metal Gate Devices for (Sub-)22nm Technology Nodes

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Abstract

In this work we provide a comprehensive evaluation of a novel, low-resistance Co-Al alloy *vs.* W to fill aggressively scaled gates with high aspect-ratios (H_{gate}~50-60nm, L_{gate}≥20-25nm). We demonstrate that, with careful liner/barrier materials selection and tuning, well-behaved devices are obtained, showing: tight R_{gate} distributions down to L_{gate}~20nm, low-V_T values, comparable DC and BTI behavior, and improved RF response. The impact of fill-metals intrinsic stress, including presence of occasional voids in narrow W-gates, on fabrication and performance is also explored.

Introduction

A low resistivity gate fill-metal is important to minimize parasitic gate resistance and to maximize performance, with variability control being key to meet the ever-increasingly stability challenges faced by scaled device circuits. Al-based metals have been successfully implemented as gate fill-metal in replacement high-k/metal gate (RMG) devices manufacturing (L_{gate} down to ~30nm) [1,2], with Ti [3-5] and more recently Co [5,6] reported as suitable wetting layers for Al to reflow, voids-free, into the gate trenches. W-filled RMG devices have also been demonstrated [7], and we will further explore in this work W potential to allow further options for channel stress enhancement thanks to its high intrinsic stress. Shrinking CDs and higher aspect-ratios (AR) for advanced nodes RMG gates represent a critical challenge for fill-gate metallization to enable further scaling. It is in this context that we will provide here an evaluation of W *vs.* Co-Al as gate fill-metal.

Device fabrication

The process flow used for device fabrication is illustrated in Fig.1 [6,7]. Silicide in source/drain (S/D) areas is formed after RMG module to allow introduction of higher thermal budgets during/after gate stack deposition. (ALD→CVD)-W or HP-PVD Al [using a low-temperature (400°C) reflow and combined with different liner/barrier layers: CVD-Co wetting layer and/or TaN] are used as fill-metals (Fig.2) in high-k last (RMG-HKL) devices, which previously got similar IL-SiO_2/HfO_2 processing and ~4nm ALD-TiN as (p-EWF)-metal (EOT~0.9-1nm).

Results & discussion

Fig.3 shows that, contrary to Al films which have insignificant stress values, W films exhibit high intrinsic stress, as measured on blanket wafers, increasing exponentially with decreasing W thickness, and more rapidly so if the films are thinned down by CMP or dry etch-back. This brings added complexity to the W-CMP of gates in RMG flow but, as shown in Fig.4, it can be used to increase the stress in the channel and boost mobility and performance, even if/when the gates are not W-voids free.

Fig.5 shows gate resistance (R_{gate}) dependence on gate CD for W- *vs.* Al-filled gate devices. Whereas for large devices R_{gate} is considerably lower for Al-filled gates, as expected from the lower Al films resistivity, the difference with regards to W-gates decreases substantially for smaller devices. This is due to alloying between the Al-fill and the previously deposited liner/wetting layer (Co), as confirmed by physical analysis (TEM, EDS/EELS, HAADF- and DF-STEM results in Figs.6,7). EDS/EELS show Co fully diffuses/intermixes with Al, being homogenously distributed in narrow gates and being detected only at the bottom and likely also at the sidewalls in larger gates (~13% Co, 87% Al in the narrow trenches, and ~10% (0%) Co at the bottom (top) of the wide trenches in Fig.7). FFT patterns obtained from high-resolution TEM images can be indexed with a mixture of Co-Al alloys and Al (e.g., Al and Co_2Al_5 in Fig.7), and the results are consistent with HAADF-STEM if projection overlap with grains of different composition occurs. Fig.6 also shows no Al/Co diffusion from the fill-metal into the HfO_2/TiN stack present underneath a TaN layer. Fig.8 shows that conductance of Al films decreases with addition of a Co-wetting layer, further decreasing with subsequent anneals, and indicative of the higher resistivity of favored Co-Al alloy phases. Highly conductive Al grains and more resistive Co-Al alloy grains therefore determine the conduction path in Al-filled gates, the proportion of which is determined by the gates CD and AR. Fig.9 shows that, by careful optimization of process conditions and layers thicknesses, Al enables tighter R_{gate} distributions down to ~20-25nm wide gates which is demonstrative of the good filling properties of Al with a Co-wetting layer, whereas occasional voids in narrow W-gates or/and W-grains size are thought to be responsible for increased R_{gate} non-uniformity. Al-liner/barrier tuning is also critical to prevent impacting the EWF-metal underneath from alloying/Al diffusion into it, with $J_G(L_{gate})$ indicating no impact on HfO_2 (Fig.10). Figs.11,12 show that if no Co-layer is used prior to Al-fill, whereas low R_{gate} is still obtained in large devices, a sharp increase in R_{gate} occurs for narrower gates due to poor filling, and even 2nm ALD-TaN covering the EWF-metal (ALD-TiN) are not effective to prevent Al diffusion into it, as assessed by ΔV_T (Al-rich TiN ⇔ more n-type EWF [7]). A scaled Co-wetting layer is important to minimize the R_{gate} increase associated with Co-Al alloy formation, while keeping good filling capabilities for narrow, high AR, gate trenches. Overall, Figs.11,12 show that the best filling and diffusion control properties in RMG-HKL devices are obtained with a TaN/Co bilayer inserted in the gate stack after EWF-metal (ALD-TiN) and prior to HP-PVD Al depositions. Fig.13 shows that TaN can be successfully introduced in the gate stack of RMG-HKL planar devices to act as an Al diffusion barrier using PVD or ALD deposition techniques. Careful TaN thickness tuning is required when using PVD to compensate for this technique's high dependence on the AR of trenches, and control the layer thickness obtained at the bottom of gate trenches (see Fig.14). Interestingly, improved RF performance was measured for RMG-HKL devices with gate stack consisting of: IL-SiO_2 / HfO_2 / EWF=ALD-TiN / ALD-TaN / in-situ (CVD-Co → HP-PVD Al), as shown in Fig.15, in comparison with Al- and W-filled gate devices without a TaN layer in the gate stack. The two Al-filled gates type of devices show similar R_{gate} values, lower than those of W-filled gates for the device dimensions (L_{gate}~0.22μm, W=10μm) plotted in Fig.15. The improved RF behavior is therefore believed to be due to the presence of a higher conductive path in the vertical direction through the gate stack, corresponding to the pilling up of layers and interfaces that are overall less resistive, possibly with TaN helping to control oxygen diffusion into the underneath TiN before/during/after Al-filling. At the same time, these devices show comparable DC and BTI behavior, indicative of similar interface states and traps in the stack (Fig.16).

Conclusions

A thorough evaluation of a novel Co-Al alloy *vs.* W to fill aggressively scaled gates with high aspect-ratios showed that, with careful liner/barrier materials selection and tuning: tight R_{gate} distributions down to L_{gate}~20nm, low-V_T values, comparable DC and BTI behavior, and improved RF response can be obtained with (Co-Al)-filled gates. At the same time, W high intrinsic stress may be used to increase the stress in the channel and boost performance for RMG devices, even if/when the gates are not W-voids free.

References

[1] K. Mistry *et al.*, IEDM *Tech. Dig.* 2007, 247; [2] P. Packan *et al.*, IEDM *Tech. Dig.* 2009, 659; [3] S. Hui *et al.*, SPIE *Proc.* 1997, Vol.3214, 79; [4] S. Kesapragada *et al.*, ASMC *Tech. Dig.* 2010, 256; [5] K. Xu *et al.*, MRS *Proc.* 2012, 1372-s3-14; [6] A. Veloso *et al.*, VLSI *Tech. Dig.* 2012 (to be published); [7] A. Veloso *et al.*, VLSI *Tech. Dig.* 2011, 34.

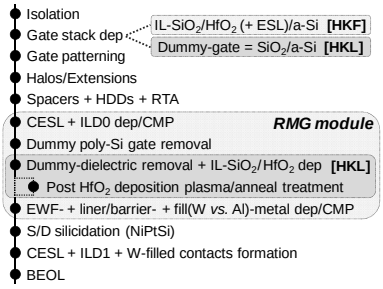

Fig.1 – Schematics of process flow used for fabrication of replacement high-k/metal gate (RMG) devices: high-k first (HKF) or high-k last (HKL). This work focus on RMG-HKL, but results are also valid for RMG-HKF.

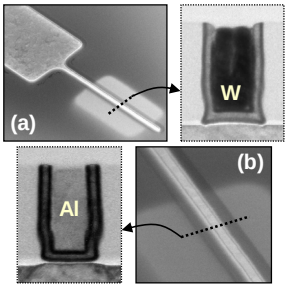

Fig.2 – SEM and TEM images of RMG-HKL devices with: a) W-filled gates, and b) Al-filled gates.

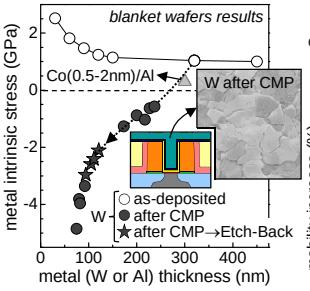

Fig.3 – W films intrinsic stress increases exponentially with decreasing W thickness, more so if films are thinned down by CMP or dry-etch. In contrast, Al films have insignificant intrinsic stress values.

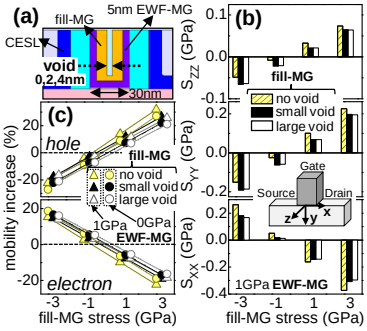

Fig.4 – The impact of voids in the fill-metal (e.g.,W) on the final stress induced in the channel is simulated using structure in (a). Results are shown in (b) for fill-metals with different intrinsic stresses, with mobility calculations in (c).

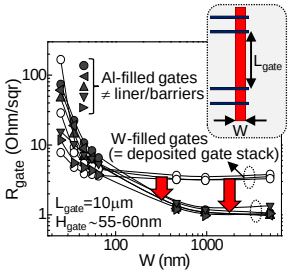

Fig.5 – For large devices R_{gate} is considerably lower (up to 3.6×) for Al-filled gates, as expected from Al films lower resistivity. However, ΔR_{gate}(Al- *vs.* W-filled gates) decreases substantially for smaller devices.

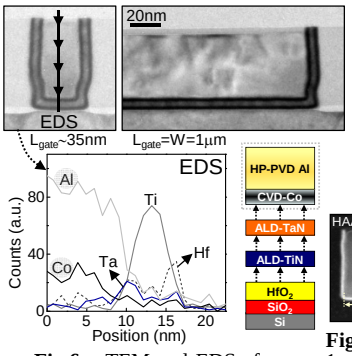

Fig.6 – TEM and EDS after full device fabrication show that Co fully diffuses into the Al fill-metal for large and small L_{gate},W_{gate} devices.

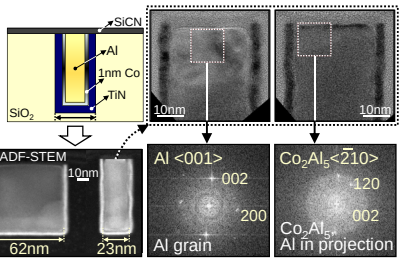

Fig.7 – Physical analysis done after depositing 1nm CVD-Co→HP-PVD Al for filling trenches with various aspect-ratios show that Co diffuses/reacts in/with Al, resulting in the formation of Al_xCo_y-alloys grains or Co-doped Al grains. Higher amount of Co detected in narrow trenches.

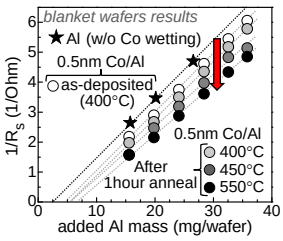

Fig.8 – Conductance of Al films after deposition by HP-PVD and subsequent anneals, with or without a CVD-Co wetting layer. Co is used to enable Al reflow in narrow trenches.

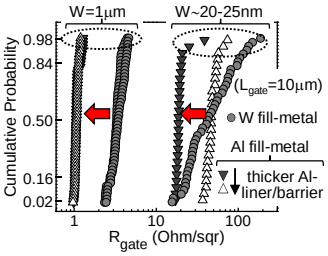

Fig.9 – Gate resistance with W *vs.* Al (& different liner/barriers) as fill-metal. Al enables tighter R_{gate} distributions down to ~20nm wide gates, whereas R_{gate} non-uniformity increases for narrow W-filled gates.

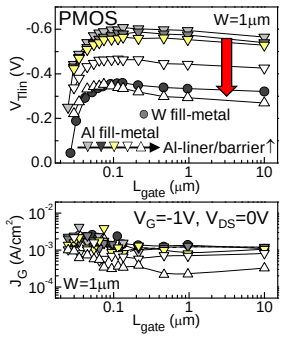

Fig.10 – Good V_T, J_G *vs.* L_{gate} control for both W- and Al-filled gates. For the latter, an optimized Al-liner/barrier is required to prevent Al diffusion/alloying into the EWF-metal underneath.

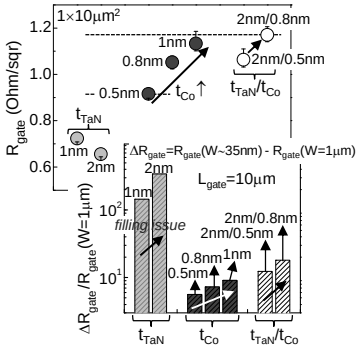

Fig.11 – Impact on R_{gate} of introducing different layer(s) in the gate stack, immediately after the EWF-metal deposition (ALD-TiN) and prior to the HP-PVD Al fill-metal: TaN, Co, and TaN→Co layers.

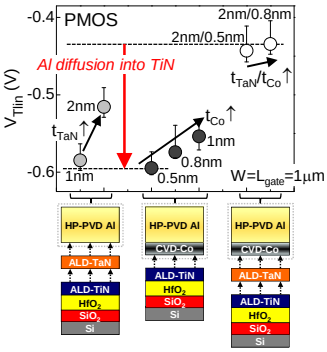

Fig.12 – Al diffusion from fill-metal into underneath EWF-metal (TiN) is assessed by ΔV_T. TaN, Co, and TaN→Co layers deposited after TiN and prior to Al-fill are compared.

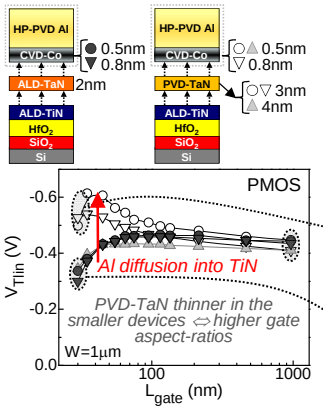

Fig.13 – Introducing a PVD-TaN layer (instead of ALD-TaN) in the gate stack prior to Co/Al-fill can also be effective to prevent V_T shifts due to Al diffusion. TaN thickness tuning is needed to compensate for PVD AR (L_{gate},W-H_{gate}) dependence.

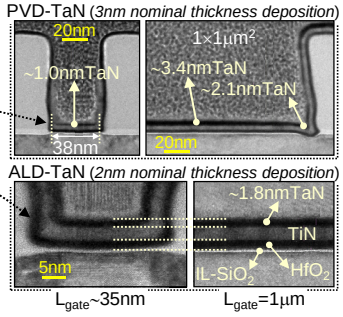

Fig.14 – TEM images show thickness of TaN layer at the bottom of gate trenches is dependent (on top) and independent (at the bottom) on the gates aspect-ratio for PVD and ALD depositions, respectively.

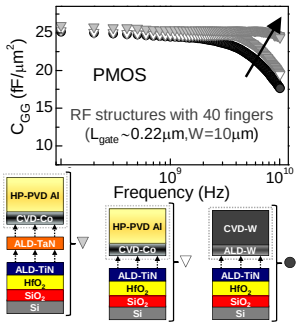

Fig.15 – Improved RF performance for Al-filled gate RMG-HKL devices, built with a TaN layer inserted in-between the EWF-metal (TiN) and Co/Al-fill.

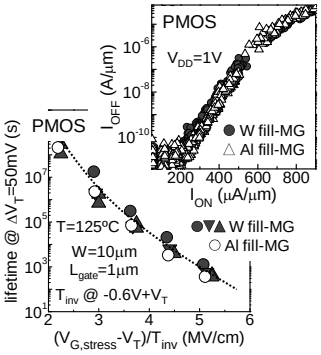

Fig.16 – Comparable DC and BTI behavior for RMG-HKL devices built with W- or Al-filled gates and similar HfO_2/TiN stack underneath. A TaN/Co bilayer was deposited prior to Al-fill.