High-Performance Tri-Gate Silicon Nanowire Transistors for Ultra-Low Power LSI
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1. Introduction
Nanowire transistors (NW Tr.) have attracted much attention as promising candidates for ultra-low power LSI [1-3]. Since NW channel is surrounded by the gate, off-current (I_{off}) is strongly suppressed. However, on-current (I_{on}) of reposted NW Tr. is low due to large parasitic resistance (R_{SD}) in S/D and degraded carrier mobility in NW channel, and systematic understanding of variability of NW Tr. is still insufficient. Towards ultra-low power LSI, I_{on} improvement and evaluation of variability and circuit performance of NW Tr. is essential.

Figs.1 illustrate the strategies to realize ultra-low voltage operation of NW Tr. in this work. We demonstrate significant I_{on} improvement of NW Tr. by stress memorization technique (SMT). Small V_{th} variations (σ_{Vth}) of NW Tr. are revealed by systematic σ_{Vth} measurement of NW Tr. with various device parameters. We also study the effects of small S factor of NW Tr. on the power consumption and performance in low-V_{dd} CMOS circuits.

2. Performance Enhancement of NW Tr. by SMT
Figs.2(a,b) show the key process sequence of tri-gate SOI NW Tr. with SMT. Raised S/D with 10nm-thick gate spacer is adopted to reduce R_{SD} [3]. Channel direction is <110> or <100>. Poly/SiO2 is used and T_{wa} is 3.5nm. For SMT, activation anneal is performed with tensile SiN on the gate structures. Fig.2(c) shows TEM after SiN removal. There are no defects due to SMT in the channel. As shown in Fig.2(d), the minimum V_{th} is around 10nm.

Fig.3 shows I_{on}-V_{th} of the fabricated NW nFETs. Significant I_{on} increase and slight V_{th} reduction are obtained by SMT. Fig.4 shows I_{on} increase ratio by SMT against W_{SD}. While ΔI_{on}/I_{on} is only 10% in planar Tr., ΔI_{on}/I_{on} rapidly increases in <110> NW Tr.

μ and R_{SD} change by SMT were extracted from R_{SD}/I_{on}. μ increase by SMT against W_{SD} is shown in Fig.5. μ increase in <110> NW nFETs is much larger than <100> nFETs. This indicates SMT induces vertical compressive strain to NW channel by suppressing the upward expansion of poly-Si gate, while longitudinal tensile strain is induced in planar Tr. (Figs.6).

Fig.7 shows R_{SG}/W_{NW} in <110> nFETs. R_{SG} largely reduces by SMT especially in narrow NW. R_{SG} of 10nm-wide NW Tr. with SMT is much lower than that earlier FinFETs [4]. In SMT process, hydrogen emitted from capping SiN diffuses to SOI/SiO2 interface and possibly generates positive fixed charges. Charges at the gate edge cause V_{th} reduction, and charges under the sidewall induce electrons in narrow S/D and reduces R_{SD} (Fig.8).

I_{on} normalized by C_{ox} is plotted against DIBL in Fig.9. I_{on}/C_{ox} of <110> SMT NW Tr. is much higher than the previous NW and SOI Tr. thanks to both μ increase and R_{SD} reduction by SMT.

3. V_{th} Variability Evaluation of NW Tr.
σ_{Vth} of tri-gate undoped NW Tr. with various L_{g} and W_{NW} were measured using 50 devices on a 300nm wafer. Fig.10 shows Pelgrom plot of NW nFETs. At each L_{g}, W_{NW} varies from 100nm to 12nm. By adopting NW circumference as the effective width (W_{eq}) in the horizontal axis, σ_{Vth} for W_{NW}=20-50nm are located on a single line with A_{eq}=0.6mV/μm irrespective of L_{g}. For W_{NW}<20nm, σ_{Vth} rapidly increases and deviates from the universal line.

σ_{Vth} universality against the channel area (L_{g}W_{NW}) indicates the parameter variations such as T_{wa}, interface-trap density (D_{IT}), or gate workfunction (WF) in the whole channel dominates σ_{Vth}. As in Fig.11, σ_{Vth} universality is valid also for shorter H_{inv} (down to 8nm) and thinner T_{wa}, indicating σ_{Vth} is not the origin of σ_{Vth}.

Fig.12(a) shows A_{σ}-W_{NW}, A_{σ} of both <110> and <100>-oriented NW nFETs is lower than planar Tr. This behavior cannot be explained by σ_{D0}, which increases with reducing W_{NW} [3]. As shown in TEM of NW channel (Fig.12(b)), grain boundaries in the gate tend to appear at NW corners. This possibly reduces σ_{D0} caused by the local effective WF variations due to pinning charges at grain boundaries randomly placed on the channel [6].

Next, the deviation from the universal line at narrow NW Tr. is studied. To study the effects of S/D on σ_{Vth}, V_{th} distribution of NW Tr. fabricated with different process (extension I/I before epi and S/D I/I after epi [7]) is shown in Fig.13. By adopting I/I after epi, the deviation from normal distribution and σ_{Vth} decrease. In I/I before epi process, crystallinity of NW extension cannot be recovered by annealing especially in narrow NW, resulting in high R_{SD} and V_{th}. As a result, W_{NW} variations due to NW LWR cause large σ_{Vth}. In contrast, good crystallinity S/D are formed and σ_{Vth} can be suppressed in I/I after epi process.

4. Low-Voltage Operation of NW CMOS Circuits
We evaluated the power consumption and performance of NW CMOS circuits by means of Spice simulation. Spice model parameters of BSIM4 [8] were extracted from NW Tr. with various L_{g} and W_{NW} in the calculation. I_{on} of all devices were set to be 50pA/μm at each V_{dd} by changing the gate work function. Fig.14 shows V_{dd} dependence of the delay time and the power consumption of NW CMOS inverter with various W_{NW}. The input operating frequency is set to be 1 GHz and fan-out is 1. The power consumption decreases with V_{dd} scaling in proportion to the square of V_{dd}. The power consumption also decreases with W_{NW} due to the reduction in the load capacitance. On the other hand, it is found that the increase of the delay is suppressed in narrower NW Tr. by low V_{dd} less than 0.7 V. In the low V_{dd} operation, the sub-threshold characteristic has a large influence on the drive current and the circuit performance. Since the ideal sub-threshold factor of NW Tr. suppresses the degradation of I_{on}/C_{ox} ratio, the delay time is kept small against V_{dd} scaling.

Fig.15 shows the power-delay product normalized by the minimum value at each W_{NW}. V_{dd} in the bottom of the power-delay product decreases with W_{NW} as a result of smaller delay time at low V_{dd}. It is also found that the curvature of the bottom region of power-delay product becomes small in narrow W_{NW}, suggesting that NW circuits have a superior immunity to V_{dd} variations.

CMOS inverter performance of NW Tr. is compared with that of bulk planar Tr. (45nm Predictive Technology Model for low power operation [9]) as shown in Fig.16. The power consumption for NW Tr. is smaller than that of bulk Tr. due to smaller C_{L} in SOI substrate. It is found that the delay time of NW Tr. is kept small at V_{dd}<0.7V thanks to smaller S factor, while the delay time of bulk Tr. rapidly increases. As a result, V_{dd} in the bottom of the power-delay product is 300mV smaller in NW Tr. than that in bulk Tr.

5. Conclusions
We demonstrated significant I_{on} improvement in SMT NW Tr. by μ increase and R_{SD} reduction. A_{σ} of NW Tr. is smaller than planar Tr. as long as R_{SD} is suppressed. Ideal subthreshold characteristics of NW Tr. combined with high I_{on} and small variability realize ultra-low power CMOS LSI.

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References
Fig. 1. (a) Schematic view of silicon nanowire Tr. fabricated in this work. (b) Strategies to realize ultra-low voltage operation of NW Tr.

Fig. 2. (a,b) Key process flow of NW Tr. with SMT. (c) TEM of NW Tr. along L direction. (d) TEM of NW under the gate along WSnw direction.

Fig. 3. Low Vth characteristics of NW nFETs with/without SMT. Significant \( I_L \) increase and slight \( \Delta V_{th} \) reduction are obtained by SMT.

Fig. 4. \( I_m \) change ratio by SMT against \( W_{Snw} \) in <110> and <100> NW nFETs. \( \Delta I_m/I_m \) rapidly increases with \( W_{Snw} \) in <110> nFETs, while it stays small in <100> nFETs.

Fig. 5. Change ratio of short-L \( \mu \) by SMT against \( W_{Snw} \) in <110> and <100> NW nFETs. \( \mu \) increase in <110> NW devices is much larger than <100> NW nFETs.

Fig. 6. Strain induced by SMT in short-L SOI planar Tr. and NW Tr.

Fig. 7. \( R_{off}W_{Snw} \) in <110> NW nFETs with/without SMT. \( R_{off} \) of narrow NW devices largely reduces by SMT.

Fig. 8. Mechanism of \( V_{th} \) and \( R_{off} \) reduction by SMT in NW Tr.

Fig. 9. \( I_m \) normalized by inversion capacitance vs. DIBL at \( L=25\mu m \). \( L_{off}/C_{inv} \) of <110> NW Tr. with SMT surpasses the previous SOI NW and planar Tr.

Fig. 10. Pelgrom plot of \( \sigma V_{th} \) of <110> NW nFETs with various \( W_{Snw} \) and \( L_m \). \( \sigma V_{th} \) for various \( W_{Snw} \) and \( L_m \) are located on a universal line with \( A_{th}=0.6mV/\mu m \) irrespective of \( L_m \).

Fig. 11. Pelgrom plot of <100> nFETs with various \( H_{fin} \) and \( T_{pol} \) and planar nFETs (\( W=1\mu m \)). \( A_{th} \) of NW Tr. is smaller than planar Tr.

Fig. 12. (a) \( A_{th}W_{Snw} \) in <110> and <100> nFETs. (b) TEM of NW under poly-Si gate. Grain boundaries in the gate tend to appear at the corners of NW.

Fig. 13. \( I_m \) distribution of NW nFETs fabricated with I/I before/after epi. The deviation from normal distribution and \( \sigma V_{th} \) decrease by I/I after epi.

Fig. 14. Delay time and power consumption of NW CMOS inverter with various \( W_{Snw} \). Inverter is composed of 1-finger NW Tr. (fan-out=1) without external load capacitance. Delay is smaller in narrower NW Tr. at low \( V_{dd} < 0.7 \) V.

Fig. 15. Normalized power delay product for different \( W_{Snw} \), where the inverter is composed of 1-finger NW Tr. (fan-out=1). \( V_{th} \) in the bottom of the power-delay product decreases with a decrease with \( W_{Snw} \).

Fig. 16. CMOS inverter performance for NW Tr. and bulk Tr. delay time, power consumption and power-delay product. \( V_{th} \) in the bottom of the power-delay product is 300mV smaller in NW Tr. than in bulk Tr.