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Extraction of Carrier Mobility in Intrinsic Channel Tri-Gate Single Silicon Nanowire MOSFETs

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1. Introduction

Along with the progress in device scaling, the nanowire MOSFET has drawn much attention recently for being promising candidate of future device structures [1-3]. To characterize the carrier transport in MOSFETs, the effective mobility μ_{eff} is one of the most important parameters. Among all the mobility measurement methods, the split C-V technique [4,5], which combines gate-to-channel capacitance C_{gc} and I_{ds} measurements, is the most fundamental one.

However, for accurate C_{gc} measurements, multiple nanowire channels have been always utilized because C_{gc} of "single" nanowire is too small to measure. This means that the reported mobility in literatures [1,6,7] has been actually an average value instead of an accurate value of individual silicon nanowire. For further investigation of mobility mechanism, the intrinsic carrier mobility of "single" silicon nanowire is strongly required.

In this work, single silicon nanowire tri-gate FETs are fabricated and compared with multiple nanowire FETs. By eliminating the effects of parasitic resistance and capacitance, the accurate mobility of single nanowire FET is directly measured by split C-V method for the first time. It is found that the electron mobility shows slight degradation while the hole mobility shows higher mobility than the universal curve.

2. Device Fabrication

Intrinsic channel tri-gate single silicon nanowire FETs in [110] channel direction are fabricated on (001) SOI wafers with T_{SOI} = 12.5nm. Fig. 1 shows a 3D schematic of device structure. The nanowire channel is patterned between large source and drain regions. The nanowire width W_{NW} is from 35nm down to 11nm. Poly Si gate and 10nm-thick SiO_2 are used as gate stacks. Multiple nanowire channel FETs, UTB FETs, and open circuit structure without channel are also fabricated on the same wafer for comparison.

3. Experiment and Results

Figs. 2 and 3 compare linear and logarithmic I_{ds}-V_{gs} characteristics of [110]/(100) nFETs with single nanowire FETs and multiple nanowire FETs with hundred channels. I_{ds} of single nanowire FETs is approximately 1/100 of that of multiple nanowire FETs. Fig. 4 shows C_{gc}-V_{gs} characteristics of nFETs with single nanowire channel. The subthreshold slope (S.S.) values are around 62mV/dec, which confirm good gate oxide interface around nanowires.

On-currents I_{on} (I_{ds} at V_{gs}=2.5V) of nanowire nFETs show a clear linear relation with the number of nanowires in the channel in Fig. 5. Fig. 6 shows on-state total resistance ($R_{on}=V_{ds}/I_{on}$) versus nanowire length in nFETs with different numbers of nanowires in the channel. The parasitic resistance can be extracted with L-array method. It is found that the influence of parasitic resistance is much weaker in longer channel with fewer nanowires. In the single nanowire nFET with a length of 53μm, the parasitic resistance is approximately 1% in the total resistance, which is negligible. Therefore, the single nanowire FET with L_{NW}=53μm is used for the mobility extraction.

On the other hand, the on-state capacitances C_{on} (C_{gc} at V_{gs}=2.5V) shown in Fig. 7 suggests the existence of serious parasitic capacitance which is mainly from the overlap part between poly Si gate and source/drain regions. Figs. 8 and 9 are the nanowire length and nanowire number dependence of on-state capacitance, respectively. The parasitic capacitance can be respectively extracted from Figs 7-9, and the extracted values are nearly the same, which means the parasitic capacitance is irrelevant to neither nanowire width/length nor nanowire number. Moreover, these parasitic capacitance values are also the same as the capacitance of an open circuit reference. So, we can remove the parasitic part by subtracting the open circuit capacitance from the nanowire nFET.

After considering the influence of both parasitic resistance and parasitic capacitance, the intrinsic carrier mobility of single nanowire FETs is extracted with a high accuracy. Fig. 10 compares extracted electron mobility of nFETs with different number of nanowires. The electron mobility in 54μm-wide UTB is in good agreement with the (100) universal curve. The lower mobility in multiple nanowire nFETs is due to larger ratio of parasitic resistance to the total resistance. Figs. 11 and 12 show electron and hole mobility in FETs with single nanowire. The mobility decreases with decreasing nanowire width for both electron and hole. It is found that hole mobility is higher than (100) universal curve even in a single nanowire FET, which originates from the effect of (110) side surface with high hole mobility.

4. Conclusions

The electron and hole mobility in "single" nanowire FETs is directly extracted from split C-V measurement for the first time. The hole mobility is higher than (100) universal curve even in a single nanowire pFET.

Acknowledgements:

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References

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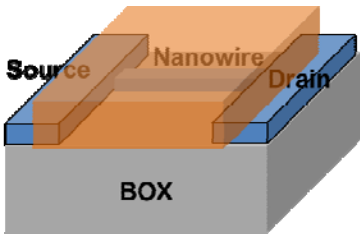

Fig.1. 3-D schematic of fabricated NW FETs.

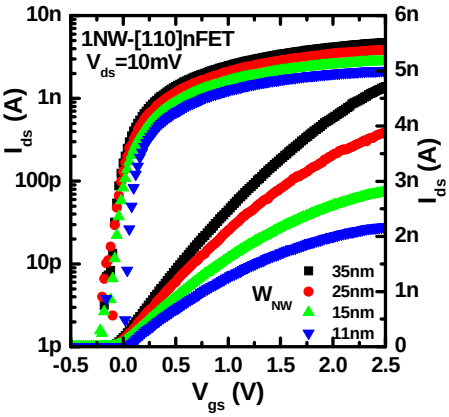

Fig.2. Measured I_{ds}-V_{gs} of single NW-nFETs.

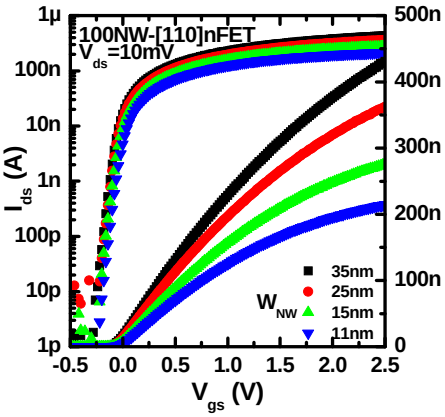

Fig.3. Measured I_{ds}-V_{gs} of 100NW-nFETs.

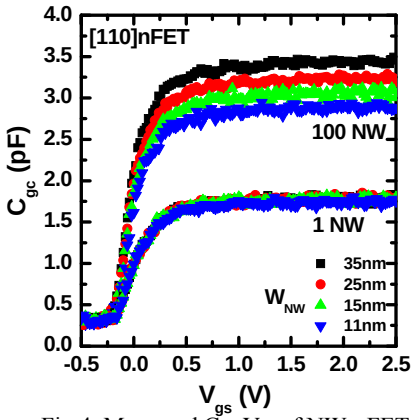

Fig.4. Measured C_{gc}-V_{gs} of NW-nFETs.

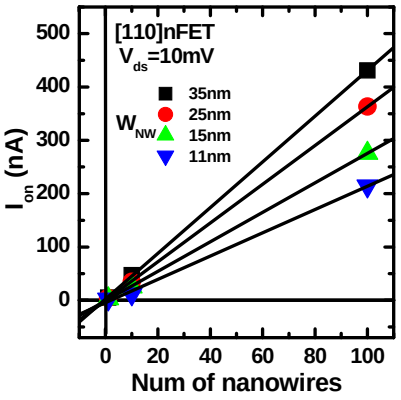

Fig.5. Nanowire number dependence of I_{on}.

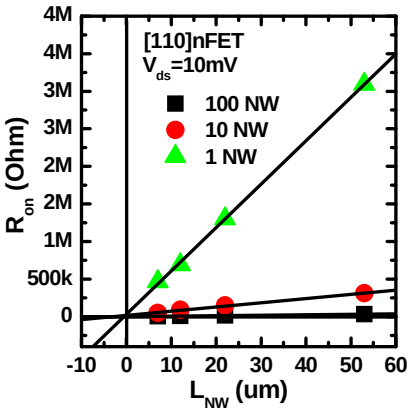

Fig.6. Nanowire length dependence of R_{on}.

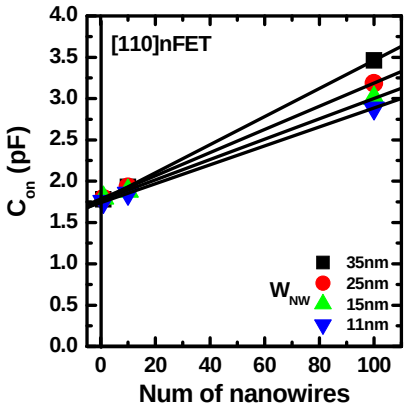

Fig.7. Nanowire number dependence of C_{on}.

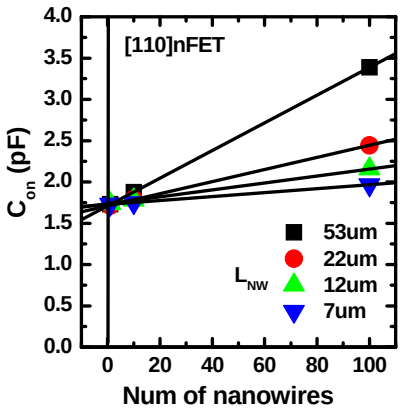

Fig.8. Nanowire number dependence of C_{on}.

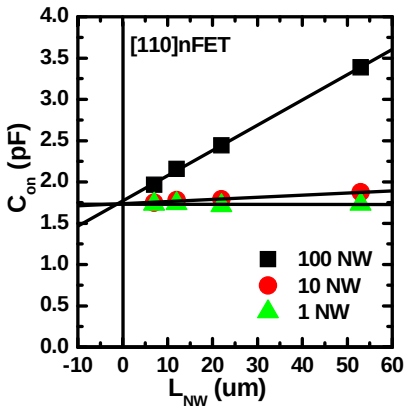

Fig.9. Nanowire length dependence of C_{on}.

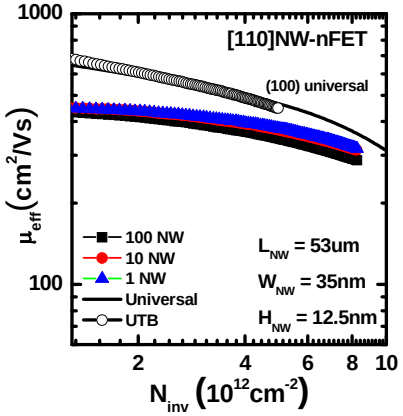

Fig.10. Electron mobility in [110] NW-nFETs.

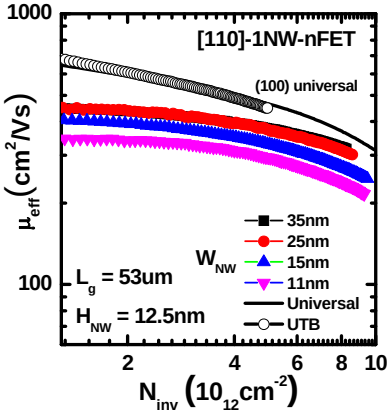

Fig.11. Electron mobility in [110] NW-nFETs.

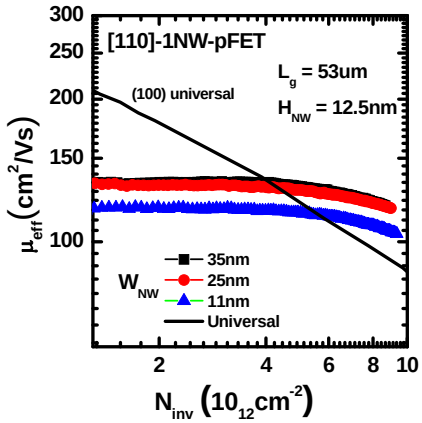

Fig.12. Hole mobility in [110] NW-pFETs.