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High performance nanoscale n-MOS gate-all-around poly-Si thin film transistors by microwave annealing

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I. Abstract

This letter introduces the nanoscale gate-all-around (GAA) n-MOS polycrystalline silicon thin-film transistors (poly-Si TFTs) by using microwave annealing (MWA) [1]-[3]. Experimental results of MWA GAA poly-Si TFTs exhibit high performance—with subthreshold slope (SS) of 105 mV/dec. and I_{on}/I_{off} ratio exceeding 107. MWA reveals the sufficient dopant activation efficiency and equivalent to rapid thermal annealing (RTA). Additionally, the short channel effect is reduced owing to the low temperature process of MWA and superior gate control of GAA structure. The proposed MWA GAA poly-Si TFT with high performance and low temperature process is promising for advanced 3D ICs.

II. Introduction

The aggressive scaling down of transistors is a recent trend, which follows Moore's law, making device physics and fabrication increasingly challenged. 3D multi-layer-stack integrated circuits (ICs), and Flash memory based on poly-Si thin-film transistor (TFT) has subsequently been introduced for high packing density and low of the interconnection delay, power consumption and cost. Previous studies have cited that microwave annealing (MWA) is a good candidate to replace RTA during the activation process for nanoscale devices and 3D ICs, owing to its ability to provide a lower process temperature for satisfactory activation and restrain the dopants diffusion. Therefore, this study investigates the poly-Si TFTs with nanoscale GAA structure and MWA. The performance of these GAA poly-Si TFTs by using MWA and RTA is compared as well.

III. Experiment

The fabrication steps are show in fig. 1 the GAA poly-Si TFTs were fabricated on a 6-inch wafer with a 400 nm-thick silicon dioxide layer. A 50 nm-thick undoped amorphous-Si layer was deposited by low-pressure chemical-vapor deposition (LPCVD) at 550 ^{o}C and solid-phase crystallized at 600 ^{o}C for 24 hours in nitrogen ambient. The active layer with ten strips of NWs was defined by electron beam (e-beam) and transferred by reactive ion etching. The samples were then dipped in a buffered oxide etch (BOE) solution for suspending NWs. An 8 nm-thick dry SiO_2 layer was grown as the tunneling oxide. Next, an in-situ doped N^+ poly-silicon by LPCVD was deposited in 250 nm, and that pattern was defined and transferred by e-beam and RIE, respectively, to form the gate electrode. The self-aligned source, drain was implanted with 15 keV phosphorous ions at a dose of 5×10^{15} cm^{-2}. Dopant activation was performed by using two methods. One sample uses MWA with a frequency of 5.8 GHz by AXOM-300 DSG Technologies, Inc [4]. The microwave power was around 2100 W for 600 sec. and the maximum processing temperature was below 500 ^{o}C under N_2 ambiance. For comparison, the other sample use conventional RTA at 1050 ^{o}C for 1 sec. A 200 nm-thick SiO_2 passivation layer was deposited. Finally, a 300 nm-thick Al-Si-Cu metallization was performed and sintered.

IV. Results and Discussion

Fig. 2a shows the top view SEM image of the GAA poly-Si TFT. Each nanowire width is 100 nm and the gate length is 42 nm. Fig. 2b exhibits the transmission electron microscopic (TEM) image of GAA poly-Si TFT. The poly-Si NW is surrounded by n^+ poly-Si gate.

Fig. 3 plots the drain current (I_d) versus gate voltage (V_g) for GAA poly-Si TFT with different gate lengths (L). Comparatively, I_d-V_g curve of the MWA device shows a high I_{on}/I_{off} current ratio (> 10^7) and steep SS (~ 105 mV/dec.). This finding reveals that the MWA can effectively activate dopants and confine dopants diffusion. Fig.4 compares the I_d-V_g curves for GAA poly-Si TFTs with MWA and RTA with the same L = 0.5 μm. Using MWA does not significantly degrade the on current. The SS (159 mV/dec.) and DIBL (0 V/V) values of MWA device are smaller than those of RTA devices.

To further elucidate the GAA gate control effect, fig. 5 compares the I_d-V_g curves of conventional planar single channel device and GAA-NW device, which were both annealed by MW. GAA device has a steeper SS (105 mV/dec.), lower DIBL and higher I_{on}/I_{off} than those of the planar single channel device. Fig. 6 compares the I_d-V_d output characteristics for GAA poly-Si TFTs with MWA and RTA, respectively. This finding reveals that the activation efficiency of RTA is slightly lower than that of MWA. Fig. 7 shows the impact of I_d-V_g curves of GAA poly-Si TFTs with MWA w/ NH_3 plasma [5] and MWA with the same L = 0.2 μm. GAA MWA w/ NH_3 plasma device has a μ_{FE} (58.01 cm^2/V_S), lower SS, lower DIBL and higher I_{on}/I_{off} than those of the GAA MWA device. Above results indicate that the MWA w/ NH_3 device has a better than the MWA device has. Fig. 8 compares the I_d-V_d output characteristics for GAA poly-Si TFTs with MWA w/ HN_3 plasma and MWA, respectively. This finding reveals that the activation efficiency of MWA is slightly lower than that of w/ NH_3 plasma.

The effective trap state density then can be obtained from the slope of the curve $\ln[I_D/(V_G-V_{FB})\ V_D]$ versus $(V_G-V_{FB})^{-2}$ as in fig. 9 [6].

Table I. compares with important parameters, and these parameters degrade as gate length decreases. GAA MWA w/ NH_3 plasma device has a μ_{FE} = 58.01 cm^2/V_S, SS = 102 mV/dec., and $I_{on}/I_{off} = 9.03\times10^8$.

V. Conclusion

This study has proposed MWA to activate GAA poly-Si TFTs, and that are compared with RTA. Experimental results indicate that MWA can confine the S/D doping profiles and maintain the activation efficiency. The feasibility of increasing the drain saturation current of MWA TFTs should be further investigated. GAA MWA poly-Si TFTs devices are studied by NH_3 plasma treatment. The hydrogen and nitrogen radicals repair the defects in the grain boundary and interface. Importantly, this study examines the feasibility of GAA poly-Si TFT with the MWA for 3D ICs owing to its high performance and low temperature process.

References

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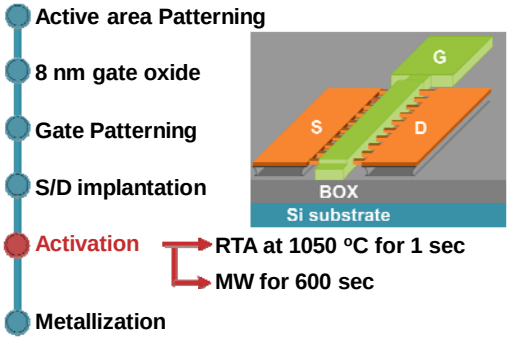

Fig. 1 The fabrication flow of GAA poly-Si TFTs device.

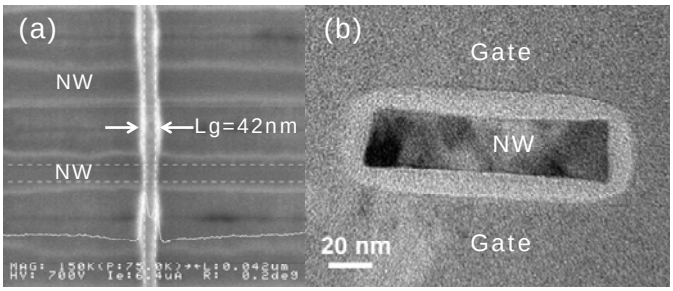

Fig. 2 (a) The SEM image of active region of GAA TFTs with gate length (L) = 42 nm. (b) Cross-section TEM image of GAA TFT.

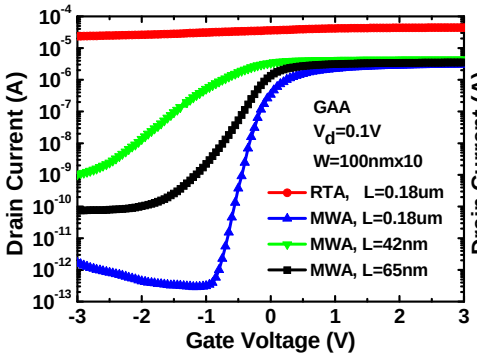

Fig. 3 I_d-V_g transfer characteristics of MWA GAA TFTs with different gate length (L) at drain voltage (V_d) = 0.1 V.

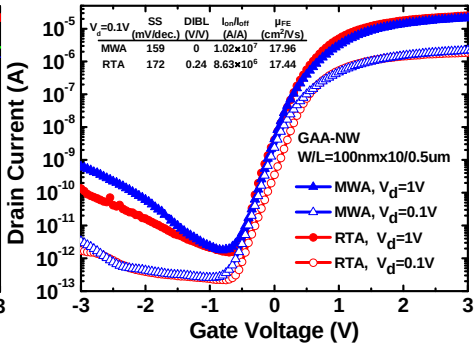

Fig. 4 Comparison of I_d-V_g transfer characteristics for MWA and RTA GAA TFTs with L = 0.5 μm.

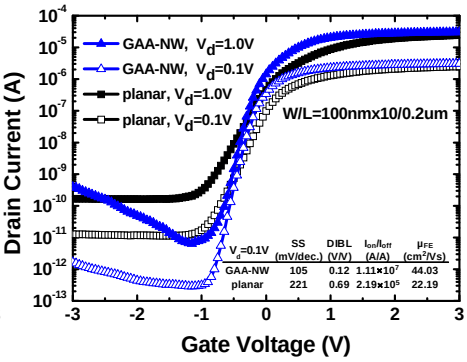

Fig. 5 Comparison of I_d-V_g transfer characteristics for planar single channel with width and GAA-NW TFTs.

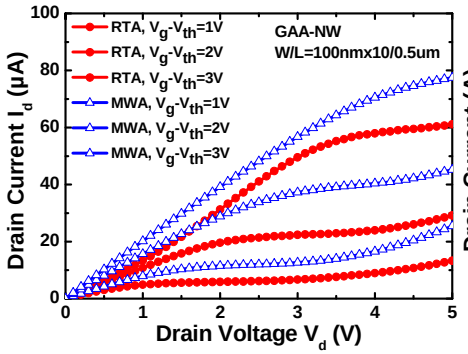

Fig. 6 Output characteristics I_d-V_d of MWA and RTA GAA TFTs with L = 0.5 μm.

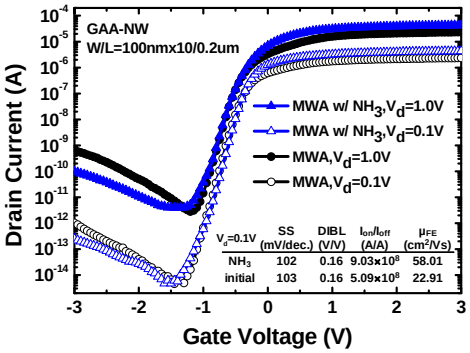

Fig. 7 I_d-V_g for GAA poly-Si TFTs with MWA w/ NH_3 and MWA with the same L = 0.2 μm.

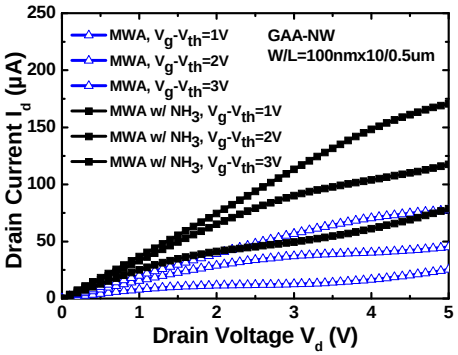

Fig. 8 Output characteristics I_d-V_d of MWA w/ HN_3 and MWA TFTs with L = 0.5 μm.

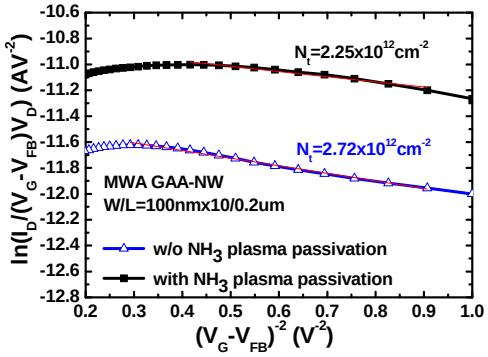

Fig. 9 Extraction of N_t plot of the MWA GAA-NW, with and without NH_3 plasma passivation.

TABLE I

Comparison of the GAA TFTs with NW-TFTs from this work to other published results.

	This work	Ref. A	Ref. B	Ref. C	Ref. D
NW cross-section	Flat Rectangle	Smooth Elliptical	Rough Triangular	Rough Triangular	Triangular
Channel structure	N-SPC GAA	N-SPC GAA	N-SPC Inverse-T	N-SPC Tri	N-SPC GAA
NH_3 Plasma	W/1hrs	W/O	W/3hrs	W/3hrs	W/3hrs
W/L (μm/μm)	0.1x10/0.2	0.03x4/0.35	0.095x2/0.8	0.136x2/1	1.2/1
EOT (nm)	8	7	20	20	25
S.S. (mV/ dec.)	102	99	90	~115	~360
I_{ON}/I_{OFF} (V_G:V_D)	>10^9 (3V;0.1V)	>10^7 (3V;1V)	>10^6 (5V;3V)	>10^6 (6V;3V)	>10^8 (10V;2V)

[A] Yi- Hsien Lu, et al.,VLSI.,pp.142,2011.[B] H.-C. Lin et al., EDL., pp. 718, 2008.
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