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Device Architectures and Their Integration Challenges for 1x nm node: FinFETs and High Mobility Channel

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1. Introduction

VLSI performance has continuously improved over past decades due to Si planar CMOS scaling. However, conventional Si planar MOSFET is coming to its scaling limit in 1x nm node. FinFET is one of the most promising device architectures for the 1x nm node, thanks to its good electro static control related to the multi gate architecture and small variability [1]. On the other hand, high mobility channel materials are attracting strong interests for further performance boost [2]. In this paper we discuss device architectures with FinFET and high mobility channel and their integration challenges for 1x nm node.

2. FinFETs integration challenges

Low external resistance (R_{ext}) is essential for high performance FinFETs. Since the fin sidewall is the main channel for FinFETs, high dopant concentration at fin sidewall is important for the low R_{ext}. Next to that, damage control of the fin doping is another important integration concern since remaining defects in the fins after junction anneal increase the fin resistance [3]. It is very challenging to get conformal doping without fin damage by conventional ion implantation (I/I), especially in dense fins [4]. Performance boost by damage-less high fin sidewall doping has been demonstrated with Self Regulatory Plasma Doping (SRPD) (fig. 1-3) [5, 6]. EOT scaling is a fundamental requirement for MOSFET scaling. Interface layer (IL) scaling by scavenging is also effective in FinFETs [7]. However, (110) sidewall channels in FinFETs cause high density of interface states and leads to severe NBTI degradation (fig. 4 and 5) [8]. One possible solution for the NBTI improvement is to introduce SiGe channel in FinFETs. The SiGe channel is effective not only for mobility improvement but also NBTI improvement when it is combined with optimized Si cap (fig. 6). [9]. The NBTI improvement can be explained by the reduced interaction between the defects in the dielectric and the channel carriers when no Si cap or a thin Si cap is used (fig. 7).

3. Challenges for high mobility channel integration

To integrate high mobility channel in a Si CMOS platform, STI etch back and selective epi (without thick buffer layers) is a promising option. With this option, defects created by the lattice mismatch between Si and the high mobility materials can be trapped at the bottom of the STI (so called Aspect Ratio Trapping (ART)) (fig. 8 (a)). By using the process flow shown in fig. 8 (b), Ge and IIIV can be co-integrated successfully (fig. 8 (c)-(f)) [10]. Gate passivation is key to reduce the interface states on the high mobility channel. Sulfur (S) passivation is effective for both Ge and InGaAs. By combining S passivation and AlO/High-k dielectric, a common gate stack integration is possible for Ge and InGaAs (fig. 9) [11].

4. Implant Free Quantum Well architecture

Strained high mobility channels are very beneficial for the device performance. We have proposed and demonstrated Implant Free Quantum Well (IFQW) architecture for strained high mobility channel [12]. Fig. 10 shows the comparison between the conventional I/I based SiGe QW device and the SiGe IFQW. IFQW features a strained high mobility QW channel and doped epi raised SD without halo I/I. Thanks to the confinement in the QW channel, IFQW shows good short channel control (fig. 11). Next to that, strained high mobility channel improves the device performance (fig. 12). The superior NBTI of SiGe channel device is confirmed also on this architecture [12]. The halo-less junction in IFQW reduces variability [13]. In-situ doped epi SD allows the use of low thermal budget processing, which suppresses the strain relaxation in high mobility channel. The IFQW architecture can be used with IIIV materials [14] and combined with the FinFET architecture. For high performance SiGe IFQW devices, the Si cap thickness on the SiGe channel (fig. 13), the thin spacer width (fig. 14) and SD strain engineering (fig. 15, 16) are very important [15, 16].

5. Conclusions

Performance boost by damage-less high fin sidewall doping is demonstrated with SRPD. IL scavenging is very effective in FinFETs EOT scaling. The SiGe channel can improve not only the hole mobility but also NBTI with optimized Si cap. Ge/IIIV co-integration is demonstrated by using ART integration scheme. S passivation and AlO/High-k enables common gate stack integration for Ge/IIIV. IFQW is a promising device architecture for high mobility channel materials.

References

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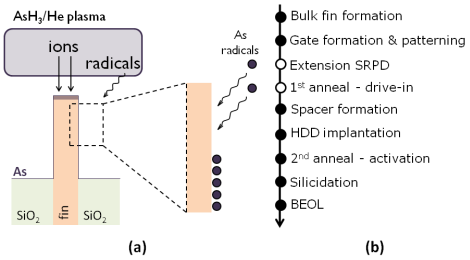


Fig. 1. (a) SRPD operation principle based on radical absorption at fin sidewall. (b) FinFET process flow for SRPD. Drive-in anneal is a key to avoid dopant loss in clean and strip.

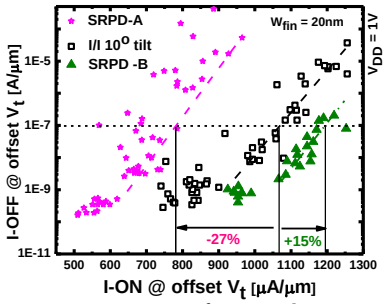


Fig. 2. N-FinFET performance boost by SRPD with optimized process A.

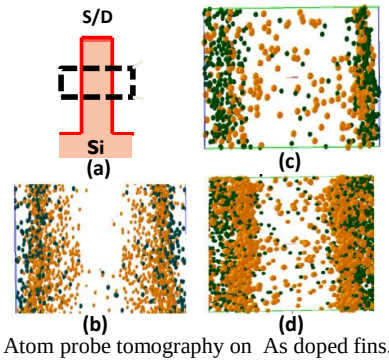


Fig. 3. Atom probe tomography on As doped fins. (a) Sample. (b) 10 degree tilt I/I. (c) SRPD-A. (d) SRPD-B.

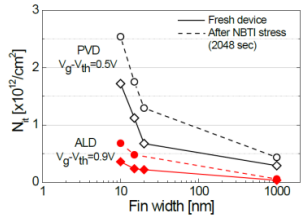


Fig. 4. Fin width dependence of interface states density. The stronger IL scavenging in PVD-TiN and (110) sidewall channel give impact on N_{it}.

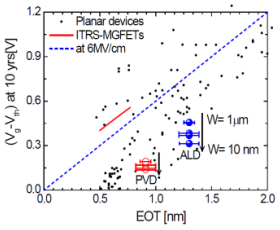


Fig. 5. NBTI impact of fin width and PVD/ALD-TiN gate.

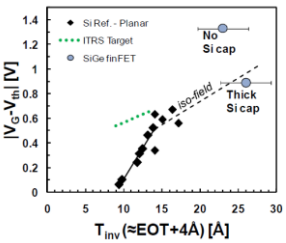


Fig. 6. NBTI improvement in SiGe channel FinFET.

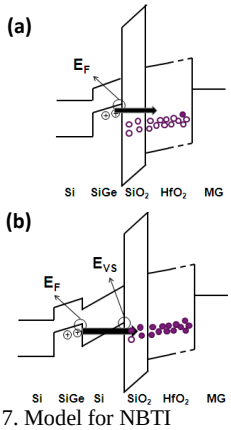
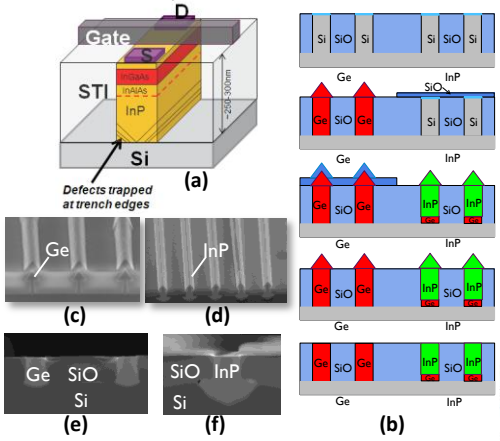


Fig. 7. Model for NBTI improvement by SiGe channel. (a) No Si cap. (b) Thick Si cap.



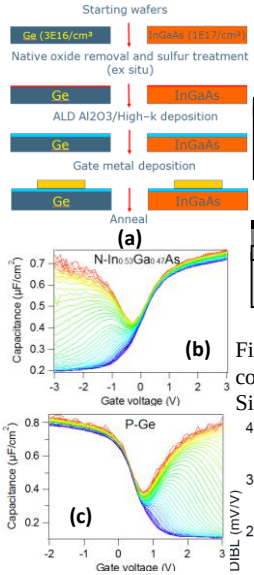


Fig. 8. High mobility material integration in Si CMOS platform. (a) Aspect Ratio Trapping. (b) Process flow for Ge/IIIV co-integration. (c)(d) Xsem after Ge and InP epi. (e)(f) Xsem after CMP

Fig. 9. (a) Common gate stack integration flow with S passivation on Ge/IIIV. (b) CV data of n-InGaAs. (c) CV data of p-Ge.

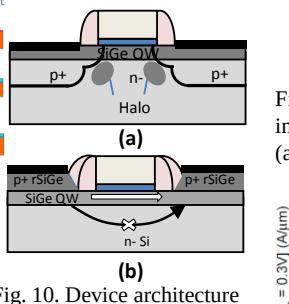


Fig. 10. Device architecture comparison. (a)Conventional SiGe QW Device. (b) IFQW.

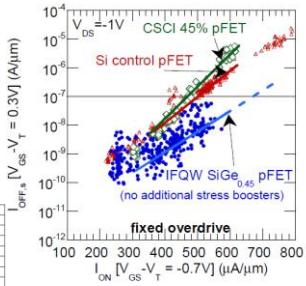


Fig. 12. Ion-Ioff comparison between conventional Si, SiGe QW (CSCI) and IFQW.

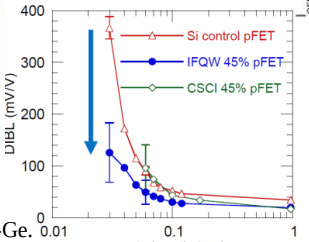


Fig. 11. DIBL comparison between conventional Si, SiGe QW (CSCI) and IFQW .

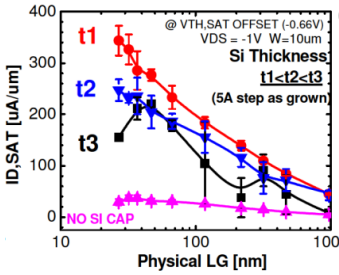


Fig. 13. Performance impact of Si cap on SiGe channel.

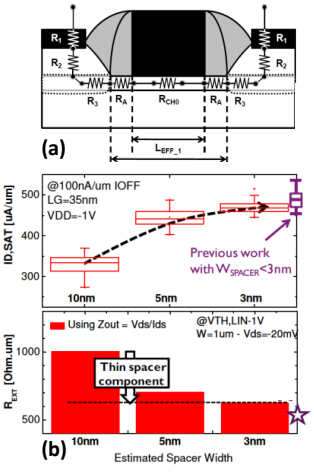


Fig. 14. (a) IFQW resist components. Thin spacer width impacts on R_A. (b) Thin spacer width impacts on Id_sat and R_{ext}.

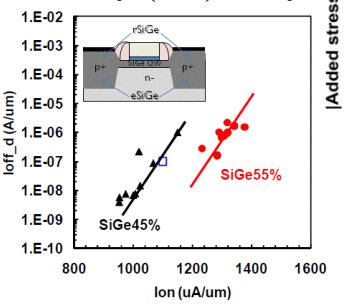


Fig. 15. High performance IFQW with eSiGe SD and optimized low temperature process.

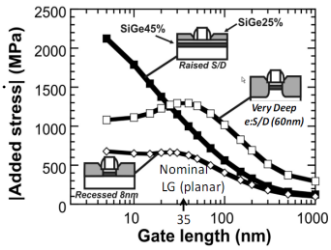


Fig. 16. IFQW SD strain engineering. For scaled gate length, raised SD is beneficial due to trade off between SD strain and channel strain relaxation by SD recess.