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Investigation and Comparison of Work Function Variation for FinFET and Ultra-Thin-Body SOI Devices Using a Voronoi Approach

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ABSTRACT

Using a novel Voronoi method that can physically consider the interaction between neighboring grains, we invesgate and compare the impact of work-function variation (WFV) on FinFET and UTB SOI devices. Our study indicates that for a given electrostatic integrity (EI) and total effective gate area, the FinFET device exhibits better immunity to WFV than the UTB SOI counterpart. We further show that, unlike other sources of random variation, the WFV cannot be supressed by EOT scaling.

I. Introduction

Random variation is a critical issue for nanoscale CMOS. Although the thinner EOT provided by high-k metal-gate can mitigate the threshold-voltage (V_{th}) variability [1], [2] from most sources of random variation (e.g., random-dopant fluctuation, line-edge roughness), the work-function variation (WFV) associated with the metal gate emerges [3]–[8]. Whether the WFV will impact the variability of FinFET and ultra-thin-body (UTB) SOI devices differently has rarely been known and merits investigation. In this work, using a novel Voronoi approach to accurately and efficiently account for the grain pattern of the metal gate, we compare the immunity of FinFET and UTB SOI devices (with the same total effective gate area) to WFV.

II. Simulation methodology

Fig 1 shows the schematic of FinFET and UTB SOI devices with the same total gate area (W_{total} = 25nm) and comparable electrostatic integrity (S.S. $\approx$ 70 mV/dec). Other pertinent device parameters are listed in TABLE I. To generate various metal-gate grain patterns for macroscopically identical devices, four factors regarding the grain should be considered: (1) $seed\ position$ (2) $shape$ (3) $size$ (4) $orientation$. In this study, our devices are designed with TiN as the gate material. Table II summarizes the two-orientation characteristic of the TiN metal gate [6].

Fig. 2(a) summarizes the flow of our proposed Voronoi methodology to simulate WFV. First, the assigned average grain size is used to estimate the number of grains (seeds) for constructing the random Voronoi grain pattern. As can be seen in Fig. 2(b), the Voronoi pattern is constructed by connecting the solid lines that are the perpendicular bisector of each dashed line. The number of black points (grain seed) in Fig. 2(b) is equal to the number of grains and randomly placed in the region. Fig. 3(a) shows the generated Voronoi pattern for the simulation of WFV in the gate region.

III. Characteristics of WFV

Based on our Voronoi approach, Fig. 4 shows the I_d-V_g dispersion for FinFET devices with WFV. As can be seen, the resulting V_{th} dispersion is asymmetric and skews at high V_{th}. The deviation from Gaussian distribution is due to the difference in the orientation probability (see Table II) of the TiN metal-gate. The orientation with larger WF possesses higher probability, thus distorting the V_{th} dispersion to higher value. Different from the method proposed in this work, the Square grain method [7] that uses the square pattern for each grain (Fig. 3(b)) is found to exhibit abrupt electric field change near the grain boundary. Fig. 5(a) shows the significant change in electric field at channel surface using the Square grain method, while the irregular grain shapes by using Voronoi method can faithfully accounts for the interaction between neighboring grains and thus smooth the electric field near the grain boundary (Fig. 5(b)).

Fig. 6 compares the V_{th} dispersion of the Voronoi and Square method for FinFET devices with various grain sizes. It can be seen that as the size of grain becomes larger, obvious discrete V_{th} dispersion is observed using the Square method whereas the Voronoi method is still able to reflect the continuous V_{th} dispersion. In addition to these two simulation approaches, a model had also been proposed to evaluate the impact of WFV in the past [8]. Fig. 7 shows a comparison of the WFV-induced V_{th} variations among the three methods. It can be seen that the model in [8] shows higher sensitivity to grain number (grain size) because it merely considers the number fluctuation, while the other two simulation methods show a saturated V_{th} variation [3] as the grain size approaches the size of device gate area.

IV. Comparison between FinFET and UTB SOI

Using our proposed Voronoi method, we investigate and compare the impact of WFV on FinFET and UTB SOI devices designed with comparable electrostatic integrity (S.S. $\approx$ 70 mV/dec) and the same total effective width (W_{total} = 25 nm). Fig. 8 compares the WFV-induced V_{th} variation between the two device structures. As can be seen, the difference increases with grain size and the UTB SOI MOSFET is shown to be more vulnerable to WFV. In the extreme case with grain size close to the device gate area, the FinFET double-gate structure possesses three possible work-function combinations (Fig. 9). For UTB device with single-gate structure, however, only two work-function combinations are allowed (Fig. 10). Therefore, the FinFET device exhibits smaller V_{th} variation and better immunity to WFV. The importance of WFV can be demonstrated Fig. 11, where Fin Line-Edge-Roughness (Fin LER) [9] is compared with WFV under various EOT. It can be seen that while the Fin-LER induced V_{th} variation can be mitigated by smaller EOT and improved EI, the impact of WFV can not be suppressed by EOT scaling. Our study may provide insights for device design in nanoscale CMOS.

Acknowledgement

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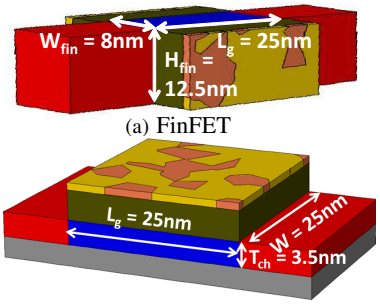


(a) FinFET

(b) UTB

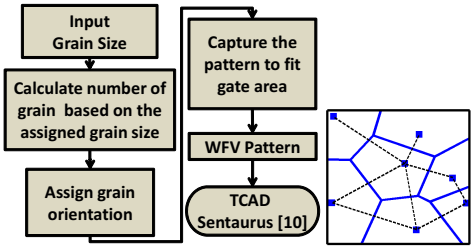
Fig. 1. Schematics of (a) FinFET, and (b) UTB devices with identical effective width.

TABLE I

UTB		FinFET	
L_g [nm]	25	L_g [nm]	25
W [nm]	25	H_{fin} [nm]	12.5
T_{ch} [nm]	3.5	W_{fin} [nm]	8
EOT [nm]	0.65	EOT [nm]	0.65
N_{ch} [cm^{-3}]	10^{17}	N_{ch} [cm^{-3}]	10^{17}

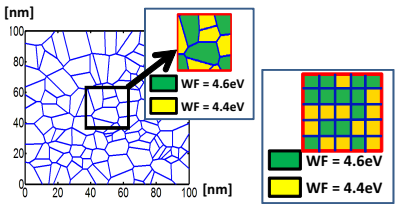
TABLE II [6]

TiN metal gate		
Orientation	<200>	<111>
WF [eV]	ψ_1 = 4.6	ψ_2 = 4.4
Probability [%]	60	40



(a) (b)

Fig. 2. (a) Flow chart for determining the WFV pattern (Number of grain = (Area)/(π × (grain size/2)^2)) (b) Formation of Voronoi pattern for WFV. The solid lines are the perpendicular bisector of dashed lines that connect each grain seed.



(a) Voronoi (b) Square

Fig. 3. Demonstration of two different simulation methods for determining the WFV pattern.

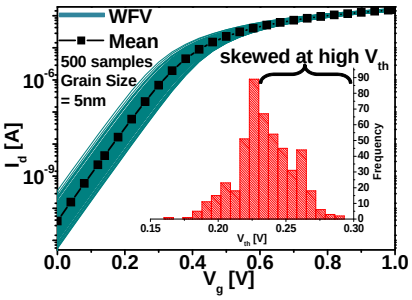


Fig. 4. The dispersion of I_d-V_g curves and skewed V_{th} distribution for FinFET with WFV.

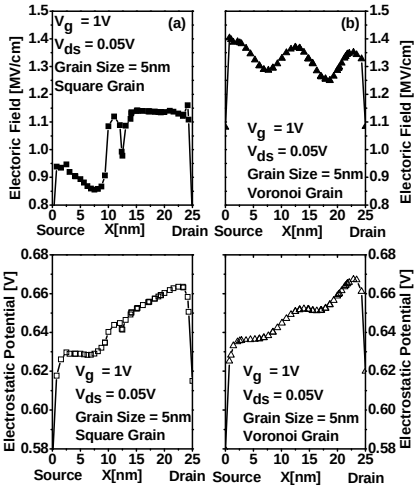


Fig. 5. Electric field and electrostatic potential at channel surface with two kinds of WFV simulation methods: (a) Square, (b) Voronoi.

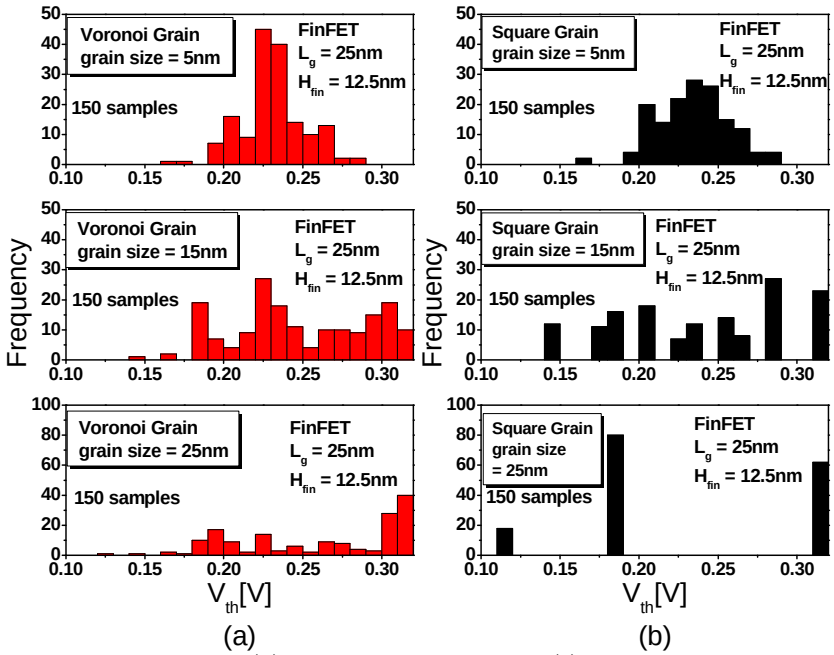


Fig. 6. V_{th} dispersion for (a) Voronoi grain method and (b) Square grain method with various grain sizes. For the cases with larger grain sizes (15nm, 25nm), obvious discrete bars are observed in (b) and shown to be physically unrealistic.

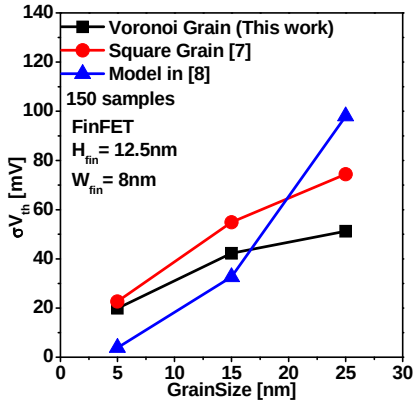


Fig. 7. Comparison of WFV-induced V_{th} variations in FinFET devices for the three methods.

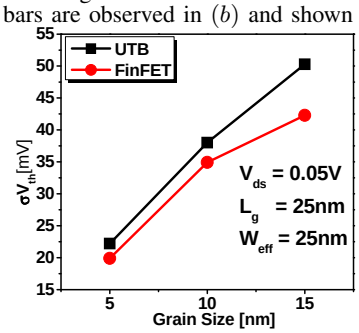
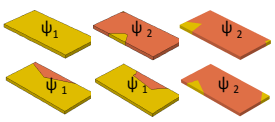
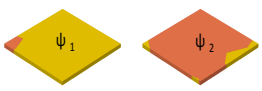


Fig. 8. Comparison of V_{th} variations for FinFET and UTB devices with various grain sizes.



(a) (b) (c)

Fig. 9. Extreme case of metal-gate patterns for FinFET: (a) both front-gate and back-gate WF = ψ_1, (b) front-gate WF = ψ_1 and back-gate side WF = ψ_2, (c) both front-gate and back-gate WF = ψ_2. Grain size = 25nm for each case.



(a) (b)

Fig. 10. Extreme case of metal gate patterns for UTB: (a) WF = ψ_1, (b) WF = ψ_2. Grain size = 25nm for each case.

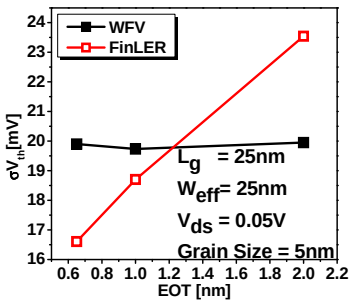


Fig. 11. Comparision of WFV and Fin-LER induced V_{th} variations for FinFET. Unlike Fin-LER, WFV can not be supressed by EOT scaling.